DOCUMENT RESUME

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IDENTIFIERS	Binary Arithmetic; Boolean Algebra; *Computer Logic; Military Curriculum Project

ABSTRACT

Targeted for grades 10 through adult, these military-developed curriculum materials consist of a student lesson book with text readings and review exercises designed to prepare electronic personnel for further training in digital techniques. Covered in the five lessons are binary arithmetic (number systems, decimal systems, the mathematical form of notation, number system conversion, mathematical operations, specially coded systems); Boolean algebra (basic functions, signal levels, application of Boolean algebra, Boolean equations, drawing logic diagrams, theorems and truth tables, simplifying Boolean equations); logic gates (diode logic circuits, transistor logic circuits, NOT circuits, EXCLUSIVE OR circuits, operational analysis); logic flip-flops, circuits, and magnetic cores; and logic circuits (counters, registers, adders, decoders, and analog-to-digital encoders). The lessons are designed for student self-study and present basic information concerning computer logic and electronic maintenance. (MN)

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MILITARY CURRICULUM MATERIALS

The military-developed curriculum materials in this course package were selected by the National Center for Research in Vocational Education Military Curriculum Project for dissemination to the six regional Curriculum Coordination Centers and other instructional materials agencies. The purpose of disseminating these courses was to make curriculum materials developed by the military more accessible to vocational educators in the civilian setting.

The course materials were acquired, evaluated by project staff and practitioners in the field, and prepared for dissemination. Materials which were specific to the military were deleted, copyrighted materials were either omitted or approval for their use was obtained. These course packages contain curriculum resource materials which can be adapted to support vocational instruction and curriculum development.

The National Center Mission Statement

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- Developing educational programs and products
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Military Curriculum Materials
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Military Curriculum Materials for Vocational and Technical Education

Information and Field
Services Division

The National Center for Research
in Vocational Education

Military Curriculum Materials Dissemination Is . . .

an activity to increase the accessibility of military-developed curriculum materials to vocational and technical educators.

This project, funded by the U.S. Office of Education, includes the identification and acquisition of curriculum materials in print form from the Coast Guard, Air Force, Army, Marine Corps and Navy.

Access to military curriculum materials is provided through a "Joint Memorandum of Understanding" between the U.S. Office of Education and the Department of Defense.

The acquired materials are reviewed by staff and subject matter specialists, and courses deemed applicable to vocational and technical education are selected for dissemination.

The National Center for Research in Vocational Education is the U.S. Office of Education's designated representative to acquire the materials and conduct the project activities.

Project Staff:

Wesley E. Budke, Ph.D., Director
National Center Clearinghouse

Shirley A. Chase, Ph.D.
Project Director

What Materials Are Available?

One hundred twenty courses on microfiche (thirteen in paper form) and descriptions of each have been provided to the vocational Curriculum Coordination Centers and other instructional materials agencies for dissemination.

Course materials include programmed instruction, curriculum outlines, instructor guides, student workbooks and technical manuals.

The 120 courses represent the following sixteen vocational subject areas:

- Agriculture
- Aviation
- Building & Construction Trades
- Clerical Occupations
- Communications
- Drafting
- Electronics
- Engine Mechanics
- Food Service
- Health
- Heating & Air Conditioning
- Machine Shop
- Management & Supervision
- Meteorology & Navigation
- Photography
- Public Service

The number of courses and the subject areas represented will expand as additional materials with application to vocational and technical education are identified and selected for dissemination.

How Can These Materials Be Obtained?

Contact the Curriculum Coordination Center in your region for information on obtaining materials (e.g., availability and cost). They will respond to your request directly or refer you to an instructional materials agency closer to you.

CURRICULUM COORDINATION CENTERS

EAST CENTRAL
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Springfield, IL 62777
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FUNDAMENTALS OF DIGITAL LOGIC

Table of Contents

Course Description Page 1

Fundamentals of Digital Logic - Text Material

Chapter 1 - Binary Arithmethic Page 7
Chapter 2 - Boolean Algebra Page 25
Chapter 3 - Logic Gates Page 47
Chapter 4 - Logic Flip-Flops Page 65
Chapter 5 - Nonlogic Circuits Page 74
Chapter 6 - Magnetic Cores Page 83
Chapter 7 - Logic Circuits Page 92

Fundamentals of Digital Logic - Lesson Assignments Page 117

FUNDAMENTALS OF DIGITAL LOGIC

Correspondence Course 7-1

Developed by:

United States Marine Corps

Development and Review Dates

February 1975

Occupational Area:

Electronics

Cost:	**Print Pages:**
$2.75	137

Availability:
Military Curriculum Project, The Center for Vocational Education, 1960 Kenny Rd., Columbus, OH 43210

Suggested Background:

Previous knowledge of transistors

Target Audiences:

Grades 10-adult

Organization of Materials:

Student lesson book with text readings, review exercises

Type of Instruction:

Individualized, self-paced

Type of Materials:	**No. of Pages:**	**Average Completion Time:**
Fundamentals of Digital Logic		
Lesson 1 – Binary Arithmetic	18	Flexible
Lesson 2 – Boolean Algebra	22	Flexible
Lesson 3 – Logic Gates	19	Flexible
Lesson 4 – Logic Flip-Flops; Nonlogic Circuits; Magnetic Cores	27	Flexible
Lesson 5 – Logic Circuits	25	Flexible
Student Lesson Book	21	

Supplementary Materials Required:

None

THE CENTER FOR VOCATIONAL EDUCATION
THE OHIO STATE UNIVERSITY

Expires July 1, 1978

2

Course Description:

This course is designed to prepare electronic personnel for further training in digital techniques. It presents need-to-know information which is basic to any maintenance course on digital equipment. The course consists of five lessons.

Lesson 1 — *Binary Arithmetic* covers number systems, decimal systems, features of number systems, the mathematical form of notation, number system conversion, mathematic operations, and specially coded systems.

Lesson 2 — *Boolean Algebra* discusses basic functions, signal levels, the application of Boolean algebra, Boolean equations, drawing logic diagrams, theorems and truth tables, and simplifying Boolean equations.

Lesson 3 — *Logic Gates* explains diode logic circuits, transistor logic circuits, NOT circuits, EXCLUSIVE OR circuits, and operational analyses.

Lesson 4 — *Logic Flip-Flop; Nonlogic Circuits; Magnetic Cores* contains three sections. Section 1 discusses bistable multivibrator, flip-flop input circuitry, three-input flip-flop, and logic flip-flop with logic gate inputs. Section 2 describes the emitter follower, pulse amplifier, relay driver, level restorer, delay lines, Schmitt trigger circuit, single-shot multivibrator, and inverter. Section 3 discusses Hysteresis loop, the metallic ribbon core, and the ferrite core.

Lesson 5 — *Logic Circuits* discusses counters, registers, adders, decoders and analog-to-digital encoders.

Each lesson contains reading assignments and review exercises. No objectives or answers to the exercises are available. The course is designed for student self-study and presents basic information concerning computer logic and electronic maintenance.

MCI 28.6d

3

FUNDAMENTALS OF DIGITAL LOGIC

7-1

MARINE CORPS INSTITUTE
MARINE BARRACKS
WASHINGTON, D.C.

SOURCE MATERIALS

CDC 30554	Electronic Computer Systems Repairman, Extension Course Institute, Gunther AFB, Ala
NAVPERS 92845	Special Technology Course, U.S. Naval Guided Missiles School, Dam Neck, Va, May 1964
NAVPERS 92901	Boolean Algebra, Bureau of Naval Personnel, June 1964
	Digest, Naval Aviation Engineering Service Unit, July 1963

5

CONTENTS

	Para	Page
Source materials		i
Table of contents		iii

Chapter 1. BINARY ARITHMETIC

	Para	Page
Introduction	1-1	1-1
Number systems	1-2	1-1
Decimal system	1-3	1-1
Features of number systems	1-4	1-2
Mathematical form of notation	1-5	1-2
Number system conversion	1-6	1-5
Mathematic operations	1-7	1-10
Specially coded systems	1-8	1-15
Summary	1-9	1-16

Chapter 2. BOOLEAN ALGEBRA

	Para	Page
Introduction	2-1	2-1
Basic functions	2-2	2-1
Signal levels	2-3	2-5
Application of Boolean algebra	2-4	2-5
Boolean equation	2-5	2-6
Drawing logic diagrams	2-6	2-7
Theorems and truth tables	2-7	2-8
Simplifying Boolean equations	2-8	2-16
Summary	2-9	2-21

Chapter 3. LOGIC GATES

	Para	Page
Introduction	3-1	3-1
Diode logic circuits	3-2	3-2
Transistor logic circuits	3-3	3-10
NOT circuits	3-4	3-17
EXCLUSIVE OR circuit	3-5	3-17
Analyses	3-6	3-18
Summary	3-7	3-19

Chapter 4. LOGIC FLIP-FLOPS

	Para	Page
Introduction	4-1	4-1
Bistable multivibrator	4-2	4-1
Flip-flop input circuitry	4-3	4-4
Three-input flip-flop	4-4	4-5
Logic flip-flop with logic gate inputs	4-5	4-7
Summary	4-6	4-9

Chapter 5. NONLOGIC CIRCUITS

	Para	Page
Introduction	5-1	5-1
Emitter follower	5-2	5-1
Pulse amplifier	5-3	5-3
Relay driver	5-4	5-4
Level restorer	5-5	5-4
Delay lines	5-6	5-5
Schmitt trigger circuit	5-7	5-6
Single-shot multivibrator	5-8	5-7
Inverter	5-9	5-8
Summary	5-10	5-9

Chapter 6. MAGNETIC CORES

Introduction 6-1 6-1
Hysteresis loop 6-2 6-1
Metallic ribbon core 6-3 6-2
Ferrite core 6-4 6-5
Summary 6-5 6-9

Chapter 7. LOGIC CIRCUITS

Introduction 7-1 7-1
Counters 7-2 7-1
Registers 7-3 7-10
Adders 7-4 7-14
Decoders 7-5 7-16
Analog-to-digital encoder 7-6 7-22
Summary 7-7 7-24

Chapter 1

BINARY ARITHMETIC

1-1. INTRODUCTION

Probably before primitive men left their caves for larger community living, they felt a need to count their animals, ornaments, and other possessions; and to keep track of how many they owned.

Later, as they lived in more complex groups, and bought, sold and bartered, their need for means of counting, measuring, computing, and recording became greater.

Man started counting with his 10 fingers, or digits (the Latin word "digitus" means finger). As long as the number he counted was 10 or less, he did well. But how could he show a number like 18? He could call in a friend to hold up 10 fingers while he held up 8. Perhaps at this point he developed the idea of equivalency, or carryover, and signified that 1 finger of his left hand equaled 5 fingers of his right hand. Thus he could hold up 3 fingers of his left hand (15) and 3 of his right hand to show 18. Perhaps he used his friend again and made his 10 fingers equal to 1 finger of his friend. Then 18 could be expressed as 1 finger of his friend and 8 of his own--a method that extended his counting ability to 11 x 10, or 110.

1-2. NUMBER SYSTEMS

a. In some ancient civilizations, man used his fingers and toes to count, and a numbering system with 20 different symbols arose. In some instances, only 5 different symbols were used.

Now many different numbering systems are possible; for example, the decimal (10-digit) system. The number of different symbols or digits used in a number system is called its base, or radix. Although any numbering system is possible that has a radix larger than 1, few systems besides the decimal system have any practical use today. These are the binary with a base of 2, the quaternary with a base of 4, and the octal with a base of 8.

b. Most digital equipment uses the binary number system because it involves only two different symbols: 0 and 1. Thus each digit of a binary number can represent a logic situation of yes or no. Since only two symbols are used, only two different signal conditions are needed to represent them. This simplifies design and improves accuracy. A large number of electronic components are 2-state (on-off) in nature; for example, a relay energized or deenergized, a vacuum tube conducting or cut off, a switch open or closed, a light bulb on or off.

1-3. DECIMAL SYSTEM

a. The decimal numbering system employs 10 different basic symbols: 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9; each of these is called a DIGIT. They are also referred to as Arabic numerals, because the Europeans adopted them from the Arabs. The Arabs, however, pointed out that their number notation system was the work of the Hindus. They did not claim to have invented it themselves. Figures or numbers without the zero were found about 300 B. C. in a cave in the hill of Mana Ghat in central India. The zero appeared about 800 years later.

b. A count using the Arabic numerals can be made up to number 9, with a different symbol to represent each different quantity. To represent a number larger than 9, place-value must be used. Place, in this case, is the position of the symbol with respect to the decimal point. It determines the power of 10 by which the digit in the place will be multiplied. (The Hindus also invented the digit place-value feature which is an important part of the decimal system.) We have become accustomed to the use of Arabic numerals in the decimal system of number notation and no doubt this system will continue to be popular for everyday use. However, our civilization is advancing rapidly in the scientific fields, and other number notation systems are finding favor in such applications as high-speed electronic devices. Therefore, it is important that we review the basic concepts of positional numbering systems using Arabic numerals so we can fully understand any system that may be employed.

1-4. FEATURES OF POSITIONAL NUMBER SYSTEMS

Three important features of positional number systems are point, place-value, and radix.

a. Point. The point is used to separate fractional parts of a number from whole parts. The point assumes the name of the number system in which it is used. That is, in the binary system it is the binary point; in the decimal system, it is the decimal point, etc.

b. Place-value. The place-value of a digit is determined by its position with respect to the point. To express the general form of a number symbolically, we use the letter D to represent any digit. Then we add a number to denote the position of the digit to the left or right of the point.

WHOLE PARTS				POINT	FRACTIONAL PARTS			
4TH DIGIT	3RD DIGIT	2ND DIGIT	1ST DIGIT	•	1ST DIGIT	2ND DIGIT	3RD DIGIT	4TH DIGIT
D4	D3	D2	D1	•	D1	D2	D3	D4

When the idea of place-value was first developed, a space was used to indicate when no quantity appeared in a place-position. For example, 205 would have been written 2 5, and 5008 would appear as 5 8- - but this could lead to confusion. Does 5 8 mean 508 or 5008? This defect led to the development of the place-holder system using a zero. Although zero has a numerical value meaning no quantity, it serves a very important function as a place-holder in modern mathematics. The idea of place-value has become very familiar to us through its use in the decimal number system; for example, 505, 5005, 50005. The zero is used for the specific function of place-holding so that the place-positions of all digits of the number are positively identified.

c. Radix or base. The radix is written as a subscript to a number. It identifies the number system and stipulates the total quantity of different Arabic numerals or symbols in that system. The radix is also referred to as the base of the number system.

When we desire to use all 10 Arabic numerals in writing any and all numbers, the radix, or base, is 10 and the decimal number system is indicated. In this system, any Arabic numeral can occur in a place-position. Examples:

$$5032_{10}, \; 2416_{10}, \; 10019_{10}, \text{ etc.}$$

Actually in order to indicate any and all quantities, we need use only the first two Arabic numerals 0 and 1. Since the quantity of different Arabic numerals used is 2, the radix, or base, is 2; and the binary number system is indicated. In this system, only a 0 or a 1 can occur in a place-position of the number. Examples:

$$11011_2, \; 10101_2, \; 1111_2, \; 101_2, \text{ etc.}$$

1-5. MATHEMATICAL FORM OF NOTATION

The following simple mathematical form is used to represent any notation system using Arabic numerals:

$$N_R = \ldots D4R^3 + D3R^2 + D2R^1 + D1R^0 + D1R^{-1} + D2R^{-2} + D3R^{-3} + D4^{-4} \ldots$$

N_R is the number. D1, D2, D3, and D4 represent digit positions 1, 2, 3, and 4, respectively, to the left or to the right of the point. R^0, R^1, R^2, and R^3 are the indicated power of the radix, representing place-values of the associated digits. This form indicates that the total number is equal to the sum of the individual digit values, with digit value being equal to the digit times the indicated power of radix.

a. Decimal system. As an example, we analyze the decimal number 5032:

The general form of any number- - - -- --------- $N_R = D4R^3 + D3R^2 + D2R^1 + D1R^0$

The general form of any decimal number -------- $N_{10} = D4(10^3) + D3(10^2) + D2(10^1) + D1(10^0)$

Which may be stated as ---------------------- $N_{10} = D4(1000) + D3(100) + D2(10) + D1(1)$

Substituting the digits of 5032 ---------------- $5032_{10} = 5(1000) + 0(100) + 3(10) + 2(1)$

Removing parentheses ------------------------ $5032_{10} = 5000 + 0 + 30 + 2$

Completing the addition ----------------------- 5032_{10}

Looking at this example, we see that:

D1 tells how many units (1's) are in the number.
D2 tells how many tens (10's) are in the number.
D3 tells how many hundreds (100's) are in the number.
D4 tells how many thousands (1000's) are in the number.

By placing the Arabic numerals 5032 in the proper place-positions in the mathematical form, we saw that the number contained 5 thousands, 0 hundreds, 3 tens, and 2 ones. In practice, we write a decimal number in its final form without resorting to the mathematical form because we have committed to memory the meaning of each place-position. However, in other number systems using Arabic numerals, you may not have committed to memory the decimal value of each place in the final form, so let us look at some examples.

b. Binary system. Instead of numbering in the familiar decimal system where place-value is indicated in powers of ten, we are numbering in the binary system whose place-value is indicated in powers of two. (Meantime, do not forget the limit placed on the quantity of different Arabic numerals permitted in the place-positions of the system chosen.) In the binary only 0 or 1 can be used as digits in the place-positions; therefore, we indicate the absence or presence of a decimal 1, 2, 4, 8, etc., by using 0 or 1 in the proper place-positions. As an example, we analyze the binary number 11001:

The general form of any number ----------------- $N_R = D5R^4 + D4R^3 + D3R^2 + D2R^1 + D1R^0$

The general form of any binary number ----------- $N_2 = D5(2^4) + D4(2^3) + D3(2^2) + D2(2^1) + D1(2^0)$

Which may be stated as ------------------------- $N_2 = D5(16) + D4(8) + D3(4) + D2(2) + D1(1)$

Substituting the digits of 11001 ------------------ $11001_2 = 1(16) + 1(8) + 0(4) + 0(2) + 1(1)$

Removing parentheses -------------------------- $11001_2 = 16 + 8 + 0 + 0 + 1$

Completing the addition ------------------------- $11001_2 = 25_{10}$

Looking at this example, we see that:

D1 tells how many ones (1's) are in the equivalent decimal number.
D2 tells how many twos (2's) are in the equivalent decimal number.
D3 tells how many fours (4's) are in the equivalent decimal number.
D4 tells how many eights (8's) are in the equivalent decimal number.
D5 tells how many sixteens (16's) are in the equivalent decimal number.

c. Octal system. Instead of numbering in the familiar ones, tens, hundreds, and thousands as in the decimal system; or in ones, twos, fours, and eights as in the binary system, we are numbering in ones, eights, sixty-fours, and five-hundred-twelves. Also, in the octal system we are limited to Arabic numerals, 0 through 7, in the place-positions. We use these numerals in proper place-positions to indicate the number of ones, eights, sixty-fours, five-hundred-twelves, etc., that are in a number.

As an example, we analyze the octal number 31.

The general form of any number---------------------- $N_R = D4R^3 + D3R^2 + D2R^1 + D1R^0$

The general form of any octal number----------------- $N_8 = D4(8^3) + D3(8^2) + D2(8^1) + D1(8^0)$

Which may be stated as------------------------------- $31_8 = D4(512) + D3(64) + D2(8) + D1(1)$

Substituting the digits of octal 31--------------------- $31_8 = 0(512) + 0(64) + 3(8) + 1(1)$

Removing parenthesis--------------------------------- $31_8 = 0 + 0 + 24 + 1$

Completing the addition------------------------------ $31_8 = 25_{10}$

Looking at this example, we see that:

D1 tells how many ones (1's) are in the equivalent decimal number.
D2 tells how many eights (8's) are in the equivalent decimal number.
D3 tells how many sixty-fours (64's) are in the equivalent decimal number.
D4 tells how many five-hundred-twelves (512's) are in the equivalent decimal number.

d. Summary. Let us write the value of decimal twenty-five in different systems, using the format in which place-values are indicated.

Binary:	2^4	2^3	2^2	2^1	2^0	(power of radix)
	16	8	4	2	1	(place-value)
N_2 =	1	1	0	0	1	= 25_{10}
Ternary:	3^4	3^3	3^2	3^1	3^0	(power of radix)
	81	27	9	3	1	(place-value)
N_3 =			2	2	1	= 25_{10}
Quaternary:	4^4	4^3	4^2	4^1	4^0	(power of radix)
	256	64	16	4	1	(place-value)
N_4 =			1	2	1	= 25_{10}
Quinary:	5^4	5^3	5^2	5^1	5^0	(power of radix)
	625	125	25	5	1	(place-value)
N_5 =			1	0	0	= 25_{10}
Sexenary:	6^4	6^3	6^2	6^1	6^0	(power of radix)
	1296	216	36	6	1	(place-value)
N_6 =				4	1	= 25_{10}
Septenary:	7^4	7^3	7^2	7^1	7^0	(power of radix)
	2401	343	49	7	1	(place-value)
N_7 =				3	4	= 25_{10}
Octal:	8^4	8^3	8^2	8^1	8^0	(power of radix)
	4096	512	64	8	1	(place-value)
N_8 =				3	1	= 25_{10}
Nonary:	9^4	9^3	9^2	9^1	9^0	(power of radix)
	6561	729	81	9	1	(place-value)
N_9 =				2	7	= 25_{10}
Decimal:	10^4	10^3	10^2	10^1	10^0	(power of radix)
	10000	1000	100	10	1	(place-value)
N_{10} =				2	5	= 25_{10}

(At this point, you should be able to recall the fundamentals of notation in numbering systems using Arabic numerals. If not, review the above points.)

1-6. NUMBER SYSTEM CONVERSION

One of the most important mathematical operations is the conversion of a number from one number system to another.

a. Decimal to any other system.

(1) To convert the whole part of a decimal number, divide the integer and each successive quotient by the radix, or base, of the new system. Continue until the quotient is 0. The remainder from the first division is the least significant digit (LSD) of the new number. The remainders from succeeding divisions are progressively more significant; the remainder from the last division is the most significant digit (MSD) of the new number.

Example: Decimal 100 conversion to

Binary

$$\begin{array}{r} 50 \\ 2\,/\,\overline{100} \\ \underline{100} \\ 0 \end{array}$$ = remainder (LSD)

$$\begin{array}{r} 25 \\ 2\,/\,\overline{50} \\ \underline{50} \\ 0 \end{array}$$ = remainder

$$\begin{array}{r} 12 \\ 2\,/\,\overline{25} \\ \underline{24} \\ 1 \end{array}$$ = remainder

$$\begin{array}{r} 6 \\ 2\,/\,\overline{12} \\ \underline{12} \\ 0 \end{array}$$ = remainder

$$\begin{array}{r} 3 \\ 2\,/\,\overline{6} \\ \underline{6} \\ 0 \end{array}$$ = remainder

$$\begin{array}{r} 1 \\ 2\,/\,\overline{3} \\ \underline{2} \\ 1 \end{array}$$ = remainder

$$\begin{array}{r} 0 \\ 2\,/\,\overline{1} \\ \underline{0} \\ 1 \end{array}$$ = remainder (MSD)

Answer: $1100100_2 = 100_{10}$

Ternary

$$\begin{array}{r} 33 \\ 3\,/\,\overline{100} \\ \underline{99} \\ 1 \end{array}$$ = remainder (LSD)

$$\begin{array}{r} 11 \\ 3\,/\,\overline{33} \\ \underline{33} \\ 0 \end{array}$$ = remainder

$$\begin{array}{r} 3 \\ 3\,/\,\overline{11} \\ \underline{9} \\ 2 \end{array}$$ = remainder

$$\begin{array}{r} 1 \\ 3\,/\,\overline{3} \\ \underline{3} \\ 0 \end{array}$$ = remainder

$$\begin{array}{r} 0 \\ 3\,/\,\overline{1} \\ \underline{0} \\ 1 \end{array}$$ = remainder (MSD)

Answer: $10201_3 = 100_{10}$

Octal

$$\begin{array}{r} 12 \\ 8\,/\,\overline{100} \\ \underline{96} \\ 4 \end{array}$$ = remainder (LSD)

$$\begin{array}{r} 1 \\ 8\,/\,\overline{12} \\ \underline{-8} \\ 4 \end{array}$$ = remainder

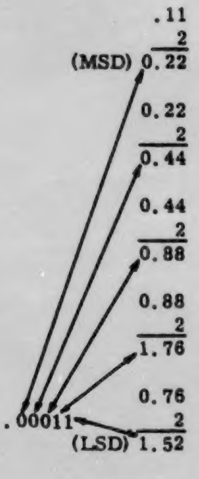
$$\begin{array}{r} 0 \\ 8\,/\,\overline{1} \\ \underline{0} \\ 1 \end{array}$$ = remainder (MSD)

Answer: $144_8 = 100_{10}$

(2) To convert the fractional part of a decimal number, multiply the given fraction and each successive product (fractional part only) by the radix, or base, of the new system. In each multiplication if a carry into the unit column (left of point) occurs, this carry is a digit of the new number; otherwise the digit is 0. The required new system of digits is obtained in order from left to right. The operation can be carried out for as many places as necessary for accuracy.

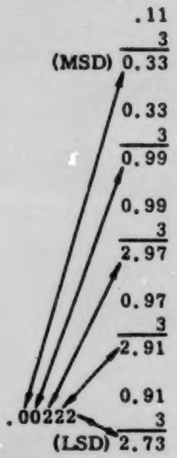
Example: Decimal 0.11 conversion to

Binary



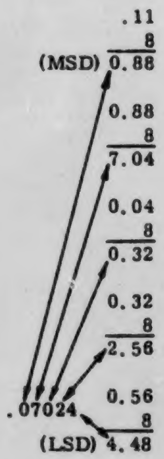
Answer: $.00011_2 = .11_{10}$

Ternary



Answer: $.00222_3 = .11_{10}$

Octal



Answer: $.07024_8 = .11_{10}$

(3) Another method of converting decimal numbers to any other system is by subtraction. It is simple when the radix is small but becomes more difficult as the radix becomes larger. This method works the same for the whole number and fractional parts of the number to be converted, as follows:

(a) Determine the largest power (place-value) of the new radix which can be subtracted from the decimal number in question. Enter a number equivalent to the number of times this place-value can be subtracted into the place-position of that power of radix.

(b) If there is a remainder, repeat step (a) using the remainder as the number in question.

(c) Continue with this procedure until the remainder is zero or until the desired accuracy has been achieved. Zeros should be entered in those place-positions where a subtraction could not be made.

Example: Decimal 100.1 conversion to binary·

2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	(power of radix)
128	64	32	16	8	4	2	1	.5	.25	.125	.0625	(place-value)
	1	1	0	0	1	0	0	.0	0	0	1	(answer)

100.1	(2^7 or 128 is too large to subtract.)
-64	(2^6 or 64 will subtract, so 1 goes in 2^6 place-position.)
36.1	
-32	(2^5 or 32 will subtract, so 1 goes in 2^5 place-position.)
4.1	(2^4 and 2^3 are each too large to subtract, so these positions are 0.)
-4	(2^2 or 4 will subtract, so 1 goes in 2^2 place-position.)
0.1	(2^1, 2^0, 2^{-1}, 2^{-2}, and 2^{-3} are each too large to subtract.)
-0.0625	(2^{-4} or .0625 will subtract, so 1 goes in 2^{-4} place-position.)
.0375	

Note: This operation could continue for any degree of accuracy required.

Example: Decimal 100.1 conversion to ternary:

3^5	3^4	3^3	3^2	3^1	3^0	3^{-1}	3^{-2}	3^{-3}	3^{-4}	(power of radix)
243	81	27	9	3	1	.333	.111	.0370	.0123	(place-value)
	1	0	2	0	1	.0	0	2	2	(answer)

100.1	(3^5 or 243 is too large to subtract.)
-81	(3^4 or 81 will subtract once, so 1 goes in 3^4 place-position.)
19.1	(3^3 or 27 is too large to subtract.)
-18	(3^2 or 9 will subtract twice, so 2 goes in 3^2 place-position.)
1.1	(3^1 or 3 is too large to subtract)
-1	(3^0 or 1 will subtract once, so 1 goes in the 3^0 place-position.)
0.1	(3^{-1} and 3^{-2} are each too large to subtract.)
-0.0740	(3^{-3} or .0370 will subtract twice, so 2 goes in 3^{-3} position.)
.0260	(3^{-4} or .0123 will subtract twice, so 2 goes in 3^{-4} position.)
-.0246	
.0014	

Exercise: Convert the following decimal numbers to a number in each of the indicated number systems. Check your answers with those on page 1-17.

Decimal	Binary	Ternary	Quinary	Octal
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				

b. Any system to decimal. To convert a number in any number system to its decimal equivalent, multiply each digit of the number by its place-value and add the products.

Example: Binary 1100100 conversion to decimal:

2^6	2^5	2^4	2^3	2^2	2^1	2^0	(power of radix)
64	32	16	8	4	2	1	(place-value)
1	1	0	0	1	0	0_2	(number to be converted)
64	+ 32	+ 0	+ 0	+ 4	+ 0	+ 0 = 100_{10}.	(answer)

Example: Ternary 10201 conversion to decimal:

3^5	3^4	3^3	3^2	3^1	3^0	(power of radix)
243	81	27	9	3	1	(place-value
	1	0	2	0	1_3	(number to be converted)
	81 +	0 +	18 +	0 +	1 = 100_{10}	(answer)

Example: Octal 144 conversion to decimal:

8^3	8^2	8^1	8^0	(power of radix)
512	64	8	1	(place-value)
	1	4	4_8	(number to be converted)
	64 +	32 +	4 = 100_{10}	(answer)

c. Binary to octal and octal to binary. Binary to octal conversion is useful because binary numbers are difficult to read and to transmit orally from one person to another, since they contain many ones and zeros. For these reasons, also to save time and reduce errors, binary numbers are often converted directly to octal numbers.

(1) A binary number is converted to an octal number by grouping the binary digits of the number into groups of three, starting at the binary point, then reading each group as a separate decimal digit. That is, each group of three binary digits is converted to a decimal form. For example, binary 101, when converted, is equal to decimal 5. In converting a group of three binary digits to a decimal digit, the highest number obtainable is 7 (111) and the lowest is 0 (000). Conversion of three binary digits to decimal form will result only in a number of some value between 0 and 7; i. e., all possible octal digits can be represented by a group of three binary digits.

Example: Binary number-------------1110101010111011_2

Binary number grouped-----(00)1 110 101 010 111 011_2

Groups to decimal--------------1 6 5 2 7 3

Octal number------------------165273_8

Note: If the left-hand group of binary digits is incomplete, zeros are added to complete the group.

(2) An octal number can be converted to a binary number by examining each octal digit separately as though it were a decimal, and indicating its equivalent binary value by a group of three binary digits. As an example, we will find the binary equivalent of octal 531. Starting with the least significant digit, octal 1 is regarded as a decimal; and grouping three binary digits to equal decimal 1 produces 001, which are the least significant three binary digits of the conversion. To find the remaining digits in order of significance, octal 3 is regarded as a decimal and the binary equivalent is 011, and octal 5's equivalent is 101. Therefore, $531_8 = 101\ 011\ 001_2$

(3) In the preceding paragraph, we examined each digit of an octal number separately as though it were a decimal digit. However, this procedure, even though correct for conversion from octal to binary, has no significance in determining the decimal value of an octal number. As previously noted, the conventional method of converting a number in any system to its decimal equivalent is to multiply each digit of the number by its place-value and to add the products obtained.

(4) It is sometimes convenient in determining the decimal equivalent of an octal number to first convert to a binary and then to a decimal number. This method is illustrated as follows:

		5			3			1	(octal)
1	0	1	0	1	1	0	0	1_2	(binary)
256	128	64	32	16	8	4	2	1	(place-value)
256 +	0 +	64 +	0 +	16 +	8 +	0 +	0 +	1 = 345_{10}	

It might also be convenient in converting decimal to binary to first convert to octal by division and then to binary. This method would require fewer divisions and save time, particularly in converting large numbers.

Exercise: Convert the following integers to a number in each of the indicated number systems. Check your answers with those on page 1-17.

Binary	Ternary	Quinary	Octal	Decimal
101	______	______	____	______
1101	______	______	____	______
111000	______	______	____	______
1100111	______	______	____	______
100001	______	______	____	______
110011	______	______	____	______
________	202	______	____	______
________	120	______	____	______
________	2021	______	____	______
________	1212	______	____	______
________	21212	______	____	______
________	222	______	____	______
________	______	100	____	______
________	______	134	____	______
________	______	413	____	______
________	______	1111	____	______
________	______	______	100	______
________	______	______	136	______
________	______	______	777	______
________	______	______	1526	______

1-7. MATHEMATIC OPERATIONS

Since practically all digital equipment uses the binary number system, study of binary arithmetic is necessary to understand its operation. A computer, in order to be versatile, must be able to perform the four basic arithmetic operations of addition, subtraction, multiplication, and division. These operations, using binary numbers, are described as follows.

a. Addition. The sum of two or more binary numbers can be determined by first converting them to decimal numbers and then performing the addition; however, this is not the method used by computers. Direct addition of binary numbers, as done in a computer, follows the rules for binary addition to give a sum and a carry as an output. These are the rules:

0+0 = 0
0+1 = 1
1+0 = 1
1+1 = 10 where the 1 is carried to the next higher column and is equal to binary 2.

Note: Once a maximum count is reached in any column (in binary counting, the maximum is 1), the next count is zero with 1 carried over to the next most significant column.

Example:

$$\begin{array}{ccccccc} D5 & D4 & D3 & D2 & D1 & & \\ & 1 & 0 & 1 & 1_2 & = & 11_{10} \\ & 1 & 1 & 1 & 0_2 & & \underline{14_{10}} \\ \hline 1 & 1 & 0 & 0 & 1_2 & & 25_{10} \end{array}$$

COLUMN D1: 1 + 0 = 1.

COLUMN D2: 1+1 = 0 carry one. In column D2 of this example, the place-value is decimal 2. That is, each binary 1 represents a decimal value of 2. Thus in column D2, binary 1 plus binary 1 means $2_{10} + 2_{10} = 4_{10}$. This sum cannot be represented in column D2 because it exceeds the place-value. However, it can be represented by a binary 1 in the next most significant column D3 because this column has a place-value of decimal four. Therefore, 0 is entered as the sum in column D2 and a binary 1 is carried over to column D3.

COLUMN D3: 0 + 1 + the 1 carried from column D2 = 0 and a carry of 1. The digits in column D3 are added: 0+1=1. This 1 must be added to the 1 which was carried in from column B. Again, the sum is 1 + 1 = 0 and 1 to carry over to the next most significant column.

COLUMN D4: 1 + 1 + the 1 carried from column D3 = 1 and a carry of 1. Again, the carry is to the next most significant column. Therefore, 1 is entered as the sum in column D4 and a binary 1 is carried over to column D5.

COLUMN D5: Since 1 has been carried in from column D4 and there are no other digits in column D5, the sum is 1+0 = 1.

The complete solution to the problem results in a sum of $11001_2 = 25_{10}$.

Exercise: Solve:

$$\begin{array}{r} 1011_2 \\ \underline{1101_2} \end{array} \quad \begin{array}{r} 1101_2 \\ \underline{1101_2} \end{array} \quad \begin{array}{r} 1111_2 \\ \underline{1111_2} \end{array} \quad \begin{array}{r} 111.111_2 \\ \underline{101.101_2} \end{array}$$

(Check your answers with those on page 1-17.)

b. Subtraction. In binary subtraction, the following basic rules apply:

$$\begin{array}{r} 0 \\ \underline{-0} \\ 0 \end{array} \quad \begin{array}{r} 1 \\ \underline{-0} \\ 1 \end{array} \quad \begin{array}{r} 1 \\ \underline{-1} \\ 0 \end{array}$$

It is frequently necessary to borrow a one (1) from the digit in one place (position) and add its equivalent value to the digit in the adjacent right place before completing the subtraction process. In binary, the process is the same as it is for decimal.

Example:

$$\begin{array}{r} 4(17) \\ \cancel{5}7 \\ -9 \\ \hline 48 \end{array}$$

We cannot subtract 9 from 7, so we borrow 1 from 5 (leaving 4), and add the equivalent value to 7, making 10+7 or 17. Now we subtract 9 from 17 to obtain a remainder of 8.

$$\begin{array}{r} 0(1+1) \\ \cancel{1}\cancel{0} \\ -1 \\ \hline 1 \end{array}$$

We cannot subtract 1 from 0, so we borrow 1 from the second place in the minuend, leaving 0(1-1=0), and add its equivalent (1+1) to the first place in the minuend. Note that there are two ones in the equivalent because, in addition, two ones were required to obtain a carry of one.

Example:

Minuend	$10110_2 = 22_{10}$
Subtrahend	$\underline{01101_2 = 13_{10}}$
Difference	$01001_2 = 9_{10}$

This problem requires borrowing in two instances. In both, the borrow is obtained from the adjacent higher order. A direct subtraction may require a borrow from a higher order which is not adjacent, as shown below:

$$\begin{array}{ccccc} & & 0\overset{1}{1}0 & & 01\overset{1}{1} \\ 100 & = & 010 & = & 011 \\ \underline{-1} & & \underline{-1} & & \underline{-1} \\ & & & & 011 \end{array}$$

Exercise: Solve:

$$\begin{array}{r} 110_2 \\ \underline{-01_2} \end{array} \qquad \begin{array}{r} 1011_2 \\ \underline{-110_2} \end{array} \qquad \begin{array}{r} 11011_2 \\ \underline{-1100_2} \end{array} \qquad \begin{array}{r} 111.111_2 \\ \underline{-101.101_2} \end{array}$$

(Check your answers with those on page 1-17.)

c. Subtraction by addition. Since most computers perform all four basic arithmetic operations by addition, the following will show how these operations are related to addition.

(1) Radix-minus-one complement. To describe how subtraction may be performed by addition, we look first at a decimal problem dealing with subtraction. The problem can be performed by taking the radix-minus-one or 9's complement of the number to be subtracted and adding it to the minuend. The radix-minus-one complement of a number is a number which, when added to the original number, results in the largest number possible in the subject number system (this number contains the same number of places as the original number). The expression, 9's complement, is sometimes used in other numbering systems, even binary, where 9 is not an admissible number. More correctly, the expression should be: radix-minus-one complement, or 1's complement.

Example:

Problem	9's Complement	Solution
$\begin{array}{r} 86 \\ \underline{-27} \\ 59 \end{array}$	$\begin{array}{r} 99 \\ \underline{-27} \\ 72 \end{array}$	$\begin{array}{r} 86 \\ \underline{+72} \\ 158 \\ \underline{\hookrightarrow 1} \\ 59 \end{array}$ (end-around-carry)

This problem is to find the difference between 86 and 27. To find the radix-minus-one complement of 27, it is necessary to subtract 27 from 99, this being the largest possible number containing the same number of places. The radix-minus-one complement of 27 is 72. The next step is to add 72 to 86, resulting in a sum of 158. When subtraction is performed by adding the radix-minus-one complement of the subtrahend, it is necessary to perform what is known as end-around-carry. This is done by removing the most significant digit of the sum and adding it to the least significant digit.

This process of subtraction through the addition of complements may seem complicated, but it lends itself readily to mechanization in a computer using the binary numbering system. To obtain the radix-minus-one complement of a binary number, simply change all 1's to 0's and all 0's to 1's.

Example:	Problem	Solution	
	$10111_2 = 23_{10}$	10111	
	$-01010_2 = 10_{10}$	+10101	(complement)
	13_{10}	101100	
		$\hookrightarrow$ 1	
		$01101_2 = 13_{10}$	

(2) True complement. Another method of complementing a number is to subtract each of its digits from the radix-minus-one of the number system and then add 1 to the least significant digit of the number formed. The number obtained by this method is known as the true complement of the number; in the decimal system it is called the 10's complement and in the binary system, the 2's complement. When subtraction is performed by adding the true complement of the subtrahend, end-around-carry is not accomplished. However, the most significant digit of the sum is dropped.

Example:	Problem	Determine the true complement.	Solution
		1111 = radix minus-one	1100_2
	$1100_2 = 12_{10}$	-0111 = subtrahend	+1001
	$-0111_2 = 7_{10}$	1000 =	Drop $\rightarrow$ $\cancel{1}0101 = 5_{10}$
	5_{10}	1 add 1	
		1001 = true complement	

Exercise: Solve by complementation:

11011_2	111001_2	110110_2	1101111_2
-01100_2	-11_2	-1001_2	-1100_2

(Check your answers with those on page 1-18.)

d. Multiplication. Multiplication by the paper-and-pencil method and the decimal system is accomplished with the aid of a muliplication table. The multiplication table for the binary system is shown in table 1-1.

Table 1-1. Rules for binary multiplication

Multiplier Digit		Multiplicand Digit		Product
0	X	0	=	0
0	X	1	=	0
1	X	0	=	0
1	X	1	=	1

Since you are familiar with the paper-and-pencil method of multiplication using decimal numbers, examples need not be given. However, this method using binary numbers is illustrated as follows:

```
Multiplicand:        1111
Multiplier:          1101
                     1111
Partial             0000
Products:          1111
                  1111
                 11000011
```

In the above example of binary multiplication, 1111 (decimal 15) is multiplied by 1101 (decimal 13) to obtain the product 11000011 (decimal 195). The partial products are equal to either zero or to the multiplicand, according to whether the corresponding multiplier digit is 0 or 1. The customary way to sum partial products is to add their digits one column at a time, starting with the lowest order. Addition of partial products is more difficult in the binary system than in the decimal system because of the carries.

When the partial products are summed in a decimal-system multiplication, the carries usually apply to the adjacent higher order column. In binary multiplication, a carry resulting from the summing of a column containing four 1's indicates an additional 1 belonging in the column two place-positions higher. This is so because in the binary system, carrying a 2(which is not a permissible digit to the adjacent higher place column) is not allowed. This problem was encountered in the preceding example.

The process of carrying over several columns often occurs in adding the partial products of a binary multiplication. This is a difficult and awkward process to execute in a computer; but it is easily avoided by adding only one partial product at a time in the formation of the final product--although such adding causes the disadvantage of having to record several intermediate sums.

Example:

Multiplicand:	1111	
Multiplier:	1101	
	1111	First partial product
	0000	Second partial product
	01111	Sum of the partial products
	1111	Third partial product
	1001011	Sum of the partial products
	1111	Fourth partial product
	11000011	Final product

Each sum of the partial products is the sum of the previous product and either the multiplicand or zero. Each succeeding addition requires that the multiplicand (or zero) be shifted to the left. The large quantity of additional circuits required to accomplish this shifting of the multiplicand dictated the use of a third method of multiplication in most digital computers.

In a computer, no multiplication table has to be stored since it is so simple and the multiplication is performed by additions and shifts, as will be illustrated in examples.

The computer method of multiplication is illustrated by adapting the previous example:

Multiplicand:	1111	
Multiplier:	1101	
	1111	First partial product
	1111	Product shifted right
	0000	Second partial product
	01111	Sum of the partial products
	01111	Sum shifted right
	1111	Third partial product
	1001011	Sum of the partial products
	1001011	Sum shifted right
	1111	Fourth partial product
	11000011	Final product

As can be seen, the final product is the same as before. The only difference between the paper-and-pencil method of multiplication and the computer method illustrated is the addition and shifting right of the partial products until the final product is obtained. This method is used in most computers because the required gate circuits are already available, since they are also required for other operations.

Exercise: Solve: $11001_2 \times 11_2$ $\quad 11011_2 \times 1100_2$ $\quad 110110_2 \times 1001_2$ $\quad 1101111_2 \times 1100_2$

(Check your answers with those on page 1-18.)

e. Division. The process of division, as accomplished by the computer, is the most time-consuming of the four arithmetic operations. Basically, it is accomplished by subtractions, shift operations, and additions, where needed.

Division can be performed by subtracting (adding complements) the divisor from the dividend repeatedly and recording the number of subtractions that were possible.

Example:

$$\begin{array}{r} 3_{10} \\ 5_{10}\,/\,\overline{15_{10}} \\ \underline{15} \\ 00 \end{array} \qquad \begin{array}{rl} 15 & \\ \underline{-5} & \text{First subtraction} \\ 10 & \\ \underline{-5} & \text{Second subtraction} \\ 5 & \\ \underline{-5} & \text{Third subtraction} \\ 0 & \text{Remainder} \end{array}$$

The same procedure is possible with binary numbers.

Example:

$$5_{10} = 101_2 \qquad 15_{10} = 1111_2$$

$$\begin{array}{r} 0011_2 = 3_{10} \\ 101_2\,/\,\overline{1111_2} \\ \underline{101} \\ 101 \\ \underline{101} \\ 000 \end{array}$$

$$\begin{array}{rl} 1111 & \\ \underline{101} & \text{First subtraction} \\ 1010 & \\ \underline{101} & \text{Second subtraction} \\ 101 & \\ \underline{101} & \text{Third subtraction} \\ 000 & \end{array}$$

Again we made three subtractions. If the number of subtractions were recorded in binary form, it would be 0011 or decimal 3. This method is not used because it is too time consuming.

Finally, let us examine how division might actually be performed by a computer. The problem is to divide 18 by 4. We first illustrate the problem, using the conventional decimal method:

$$\begin{array}{r} 4.5 \\ 4\,/\,\overline{18.0} \\ \underline{16} \\ 20 \\ \underline{20} \\ 00 \end{array}$$

Next, the steps utilized by a computer in solving this problem:

$4_{10} = 100_2$
$18_{10} = 10010_2$

			Quotient
Step 1	10010		
	100		
	10010		0 MSD
Step 2	100100	(left shift)	
	100		
	100100		0
Step 3	1001000	(left shift)	
	100		
	0001000		1
Step 4	0010000	(left shift)	
	100		
	0010000		0
Step 5	0100000	(left shift)	
	100		
	0100000		0
Step 6	1000000	(left shift)	
	100		
	0000000		1 LSD

Answer: 00100.1_2

In step 1 of the problem, MSD of the dividend and LSD of the divisor are lined up, and a subtraction is attempted. If a subtraction had been accomplished, the difference would have been a negative number. For simplicity, when a subtraction would result in a negative remainder, it is not performed, a zero is recorded in the quotient and the dividend shifted one place left for the next operation. When subtraction is accomplished, 1 is recorded in the quotient (as in steps 3 and 6). In the example, the first five places of the quotient represent a whole number, and the sixth place or LSD represents .5 which is a fraction. Here, as in any other division, when the quotient has more places than the dividend, a fractional part is indicated. To be accurate only to a whole number, the quotient contains the same number of places as the dividend.

Exercise: $11_2\ /\overline{111001_2}$ $1100_2\ /\overline{11011_2}$ $1100_2\ /\overline{1101111_2}$

(Check your answers with those on page 1-18.)

1-8. SPECIALLY CODED SYSTEMS

a. Binary coded decimal system (BCD). It is possible to group symbols to get a workable system such as the binary coded decimal or 8421 system. This system derives its name from the symbols 8, 4, 2, 1 that are the place-values of the digits in a 4-digit binary number. Instead of a true conversion to binary, this system codes each of the 10 Arabic numerals into a 4-digit binary number as follows:

Decimal Number	Binary Code
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

Decimal 25 is written 0010 0101. Decimal 291 is written 0010 1001 0001. In this system, each decimal digit is coded separately to a binary form. (Remember that the decimal number is not converted to the binary form. That is, 00100101_2 is not equal to 25_{10}. Although the 8421 code is commonly used, obviously many special codes are possible. To interpret such codes you must know the system being used.

b. Gray code system. Similar to the binary is the Gray code or reflected binary system (table 1-2). A useful application of this is found in some types of analog-to-digital conversion equipment. Its advantage is drived from the fact that successive integers differ one from the next by only one digit, thus reducing the degree of error which might occur when numbers are transferred. The usefulness to the reflected binary system does not extend to arithmetic operations. Even simple addition is relatively difficult with this system. Actual conversion to the Gray code is accomplished in the computer by the utilization of a digital logic circuit.

Table 1-2. Relationships between numbers in the decimal, binary, and Gray code systems

Decimal	Binary	Gray Code	Decimal	Binary	Gray Code
0	0000	0000	8	1000	1100
1	0001	0001	9	1001	1101
2	0010	0011	10	1010	1111
3	0011	0010	11	1011	1110
4	0100	0110	12	1100	1010
5	0101	0111	13	1101	1011
6	0110	0101	14	1110	1001
7	0111	0100	15	1111	1000

Notice in table 1-2 that a change from 0111_2 (7_{10}) to 1000_2 (8_{10}) requires a change from three ones and a zero to three zeroes and a one. Thus, all digits were changed simultaneously for a consecutive count, whereas in the Gray code system consecutive numbers differ by a change of only one digit.

c. Biquinary system. The biquinary system is a coded system similar to the abacus in that it has two sections. One section, the "bi" portion, has two places, while the other section, the "quin" portion, has five places. This system has limited use in modern equipment. It was used in earlier decimal counters to reduce from 10 to 7 the number of bistable devices necessary to count from 0 to 9. The code has a self-checking characteristic in that the biquinary representation of a decimal number always has exactly two "ones," which makes it applicable to error-detection circuits.

Table 1-3. Biquinary code with decimal equivalents

Decimal	Biquinary 50-43210 (place-value)	Decimal	Biquinary 50-43210 (place-value)
0	01 00001	5	10 00001
1	01 00010	6	10 00010
2	01 00100	7	10 00100
3	01 01000	8	10 01000
4	01 10000	9	10 10000

The biquinary code (table 1-3) is based on the idea that each digit place represents a decimal value. To find the total decimal value, the equivalent values of thos digit places occupied by ones are added. For example, the biquinary representation of the decimal number zero is 01-00001. In this case the coded value of the 1 in the "bi" portion is equal to 0; also, the coded value of the 1 in the "quin" portion, is equal to 0. Adding the value of the "bi" portion to the value of the "quin" portion, we have a sum of zero which is equal to the value of the decimal 0. As another example, the biquinary representation for the decimal number 2 is 01-00100. Here the coded value of the 1 in the "bi" portion is 0, and the coded value of the 1 in the "quin" portion is 2. Adding the coded value of the two portions, we have decimal 2.

1-9. SUMMARY

a. Digital equipment deals directly with numbers composed of digits or symbols called Arabic numerals. The binary number system is used much more than the ternary, octal, decimal, or other specially coded number systems.

b. The radix, or base, which is written as a subscript to the number, identifies the number system and tells how many different symbols or digits are used. Two other features are important in number system notation: (1) the place-value, which is the decimal value of the power of radix of the position that the digit occupies in the number; and (2) the point, which is used to separate the fractional part of a number from the whole part. The total value of a number in terms of the decimal-number system is equal to the sum of the individual digit values. The digit value is equal to the product of the digit and its place-value.

c. Most digital equipment uses the binary number system and performs all arithmetic computations by addition. This is practical because subtraction, multiplication, and division are simple variations of the basic arithmetic operation of addition. In the computer, subtraction is accomplished by addition of the minuend and a complemented subtrahend; multiplication is accomplished by a series of additions and shifts; and division becomes a series of subtractions (complement additions) and shifts.

ANSWERS TO EXERCISES

Exercise following para 1-6a:

Decimal	Binary	Ternary	Quinary	Octal
1	1	1	1	1
2	10	2	2	2
3	11	10	3	3
4	100	11	4	4
5	101	12	10	5
6	110	20	11	6
7	111	21	12	7
8	1000	22	13	10
9	1001	100	14	11
10	1010	101	20	12
11	1011	102	21	13
12	1100	110	22	14
13	1101	111	23	15
14	1110	112	24	16
15	1111	120	30	17
16	10000	121	31	20
17	10001	122	32	21
18	10010	200	33	22
19	10011	201	34	23
20	10100	202	40	24

Exercise following para 1-6c:

Binary	Ternary	Quinary	Octal	Decimal
101	12	10	5	5
1101	111	23	15	13
111000	2002	211	70	56
1100111	10211	403	147	103
100001	1020	113	41	33
110011	1220	201	63	51
10100	202	40	24	20
1111	120	30	17	15
111101	2021	221	75	61
110010	1212	200	62	50
11010100	21212	1322	324	212
11010	222	101	32	26
11001	221	100	31	25
101100	1122	134	54	44
1101100	11000	413	154	108
10011100	12210	1111	234	156
1000000	2101	224	100	64
1011110	10111	334	136	94
111111111	200221	4021	777	511
1101010110	1011122	11404	1526	854

Exercise following para 1-7a:

$$\begin{array}{r} 1011 \\ \underline{+1101} \\ 11000 \end{array} \qquad \begin{array}{r} 1101 \\ \underline{+1101} \\ 11010 \end{array} \qquad \begin{array}{r} 1111 \\ \underline{+1111} \\ 11110 \end{array} \qquad \begin{array}{r} 111.111 \\ \underline{+101.101} \\ 1101.100 \end{array}$$

Exercise following para 1-7b:

$$\begin{array}{r} 110 \\ \underline{-\ 1} \\ 101 \end{array} \qquad \begin{array}{r} 1011 \\ \underline{-110} \\ 101 \end{array} \qquad \begin{array}{r} 11011 \\ \underline{-1100} \\ 1111 \end{array} \qquad \begin{array}{r} 111.111 \\ \underline{-101.101} \\ 10.010 \end{array}$$

Exercise following para 1-7c:

$$\begin{array}{r} 11011 \\ \underline{-01100} \\ 1111 \end{array} \longrightarrow 10011 + 1 \longrightarrow \begin{array}{r} 11011 \\ \underline{+10100} \\ \cancel{1}01111 \end{array}$$

$$\begin{array}{r} 111001 \\ \underline{-000011} \\ 110110 \end{array} \longrightarrow 111100 + 1 \longrightarrow \begin{array}{r} 111001 \\ \underline{+111101} \\ \cancel{1}110110 \end{array}$$

$$\begin{array}{r} 110110 \\ \underline{-001001} \\ 101101 \end{array} \longrightarrow 110110 + 1 \longrightarrow \begin{array}{r} 110110 \\ \underline{+110111} \\ \cancel{1}101101 \end{array}$$

$$\begin{array}{r} 1101111 \\ \underline{-0001100} \\ 1100011 \end{array} \longrightarrow 1110011 + 1 \longrightarrow \begin{array}{r} 1101111 \\ \underline{+1110100} \\ \cancel{1}1100011 \end{array}$$

Exercise following para 1-7d:

$$\begin{array}{r} 11001 \\ \underline{x11} \\ 11001 \\ \underline{11001} \\ 1001011 \end{array} \qquad \begin{array}{r} 11011 \\ \underline{x1100} \\ 1101100 \\ \underline{11011} \\ 101000100 \end{array} \qquad \begin{array}{r} 110110 \\ \underline{x1001} \\ 110110 \\ \underline{110110} \\ 111100110 \end{array} \qquad \begin{array}{r} 1101111 \\ \underline{x1100} \\ 110111100 \\ \underline{1101111} \\ 10100110100 \end{array}$$

Exercise following para 1-7e:

$$\begin{array}{rr} & 10011 \\ 11 & \overline{/\,111001} \\ & \underline{11} \\ & 100 \\ & \underline{11} \\ & 11 \\ & \underline{11} \end{array} \qquad \begin{array}{rr} & 10.01 \\ 1100 & \overline{/\,11011.00} \\ & \underline{1100} \\ & 1100 \\ & \underline{1100} \end{array} \qquad \begin{array}{rr} & 1001.01 \\ 1100 & \overline{/\,1101111.00} \\ & \underline{1100} \\ & 1111 \\ & \underline{1100} \\ & 1100 \\ & \underline{1100} \end{array}$$

02

Chapter 2

BOOLEAN ALGEBRA

2-1. INTRODUCTION

a. The objective of this chapter is to explain the basic concepts of Boolean algebra so that you may understand the purpose and operation of the logic circuits used in digital equipment.

b. In 1854, George Boole, an English mathematician, published his classic, An Investigation of the Laws of Thought. His stated intention was to perform a mathematical analysis of logic. No practical use was made of this new type of logic until 1938 when C.E. Shannon, a research assistant at the Massachusetts Institute of Technology, showed that this form of algebra is useful for indicating the logical functions of telephone and computer switching circuits. Since then, the increasing need for computers and automatic-dial telephones has created a rapid growth in the application of Boolean algebra.

c. Because Boolean algebra is different from ordinary algebra, it may seem confusing at first; actually, it is not difficult. Understanding its functions will help you to understand the operation of the logic circuits used in digital equipment. However, Boolean algebra does not deal directly with electronic circuits.

2-2. BASIC FUNCTIONS

Boolean algebra expresses logical functions mathematically. Once the Boolean expression is derived, a diagram of the logical functions involved may be drawn. This logic diagram illustrates the required functions and indicates the type of electrical circuit required. An electrical circuit can then be built which will accomplish these functions. In computer design and in certain maintenance applications, Boolean expressions and logic diagrams may be used conveniently to represent electronic circuit functions without taking the time to draw the actual circuit components.

In Boolean algebra there are three basic operations: AND-ing, OR-ing, and complementation. The symbols which denote these operations do not have the same meaning as in ordinary algebra. The addition sign (+) means OR, the multiplication sign (·) means AND, and the complementation sign ($\overline{\quad}$) means inversion or NOT the signal. Note that the multiplication sign is frequently omitted, as in ordinary algebra, and the AND function is assumed. These basic functions will be discussed before considering more complex expressions.

a. The OR function. An equation in ordinary algebra such as $A + B = C$ has an infinite number of possible values, since A and B can be assigned any number. On the other hand, an equation in Boolean algebra can have only one of two possible values. All variables and constants are either 0 or 1. Therefore, in the Boolean expression, A or B equals C, there are only four possible numberical combinations, which will satisfy the following equations:

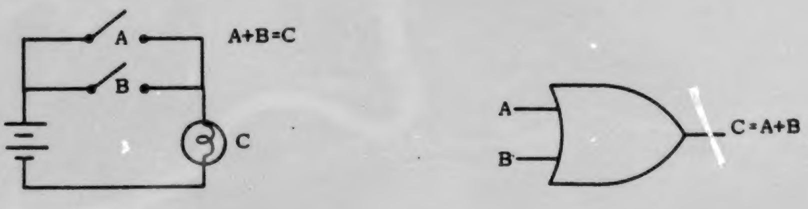
$$\begin{array}{c} A + B = C \\ 0 + 0 = 0 \\ 0 + 1 = 1 \\ 1 + 0 = 1 \\ 1 + 1 = 1 \end{array}$$

These results could represent a standard addition table, except the last entry. When both A and B are 1, the logical sum is also 1. The + symbol therefore does not have the same meaning as in ordinary algebra, but it is a logical sum symbol. It should also be noted that any number of variables can be represented in the OR equation. For instance, in the equation $W + X + Y + Z = A$, if W, X, Y, and Z all had the value of 1, the logical sum of values, or

A, would be 1. That is, if one or all of the quantities in the equation are 1, the result is 1. Conversely, the result is 0 only if all the quantities in the equation are 0.

Figure 2-1A, illustrates the OR function by the use of a simplified light-switching circuit. Figure 2-1B shows the logic symbol for this circuit, which is called an OR gate.

Note: The logic symbols in this chapter are in accordance with MIL-STD-806B.



A. Simplified circuit.

B. Logic symbol.

Fig 2-1. OR circuit.

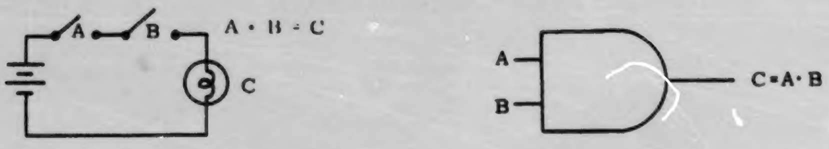
The Boolean equation for the circuit shown in figure 2-1A is $A + B = C$. Switch A and switch B may be represented by 1 when in the closed position, and by 0 when in the open position. Also, light C may be represented by 1 when it is glowing, and by 0 when it is off. When switch A is closed, the circuit is represented by the equation $1 + 0 = 1$. When switch B is closed, the circuit is represented by the equation $0 + 1 = 1$. Thus, light C will glow when either switch A or B is in the closed position. If both switches A and B are closed, the light C glows with the same intensity as it does with only one switch closed; and the circuit will be represented by the equation $1 + 1 = 1$.

b. The AND function. In ordinary algebra, the equation $A \cdot B = C$ means, A multiplied by B equals C. Because the quantities A and B can be assigned any value, the equation can have an infinite combination of numbers. However, since Boolean algebra uses only the values 1 and 0, these are the only four possible combinations which satisfy the Boolean expression A AND B equal C:

$A \cdot B = C$
$0 \cdot 0 = 0$
$0 \cdot 1 = 0$
$1 \cdot 0 = 0$
$1 \cdot 1 = 1$

In the AND equation, the result is 1 only when all the given quantities are 1. Here also, note that any number of variables can be represented in the AND equation; however, as in ordinary multiplication, the logical product will be 1 only if all of the factors are 1.

Figure 2-2A illustrates the AND function by the use of a simplified light-switching circuit. Figure 2-2B shows the logic symbol for this circuit, which is called an AND gate.



A. Simplified circuit.

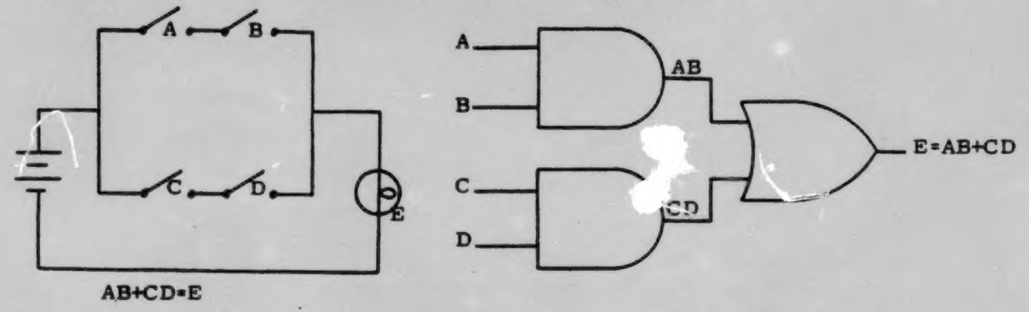
B. Logic symbol.

Fig 2-2. AND circuit.

The Boolean equation for this circuit is A · B = C. Light C will glow if switches A and B are in the closed position. The closed position for either switch may be represented by 1; and the open position of either, by 0. Also, light C may be represented by 1 when it glows, and by 0 when it is off. When switches A and B are arranged in the four possible combinations previously given, in only one case will the light C glow; that is, when switches A and B are closed. This condition is represented by the equation 1 · 1 = 1.

Note: In many equations the AND sign (·) may not be expressed. Nevertheless, it is assumed to be there. For example: A = CD.

c. Combination AND-OR functions. Complex switching networks are frequently required to perform a combination of logical functions. Figure 2-3A shows a circuit in which light E will glow when switches A and B or C and D are closed, that is, an OR function combined with two AND functions. The Boolean equation for this circuit is AB + CD = E, and is read A AND B OR C AND D equal E. The logic diagram for the circuit is given in figure 2-3B.

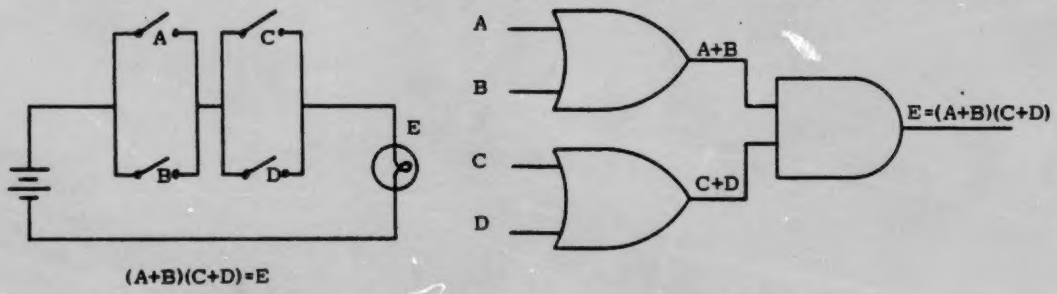


A. Simplified circuit.

B. Logic diagram.

Fig 2-3. Combination AND-OR circuit.

Figure 2-4A shows a simplified light-switching circuit in which two OR functions are combined with an AND function. The equation for this circuit is (A + B) (C + D) = E, and is read A OR B AND C OR D equal E. The logic diagram for this circuit is shown in figure 2-4B.



A. Simplified circuit.

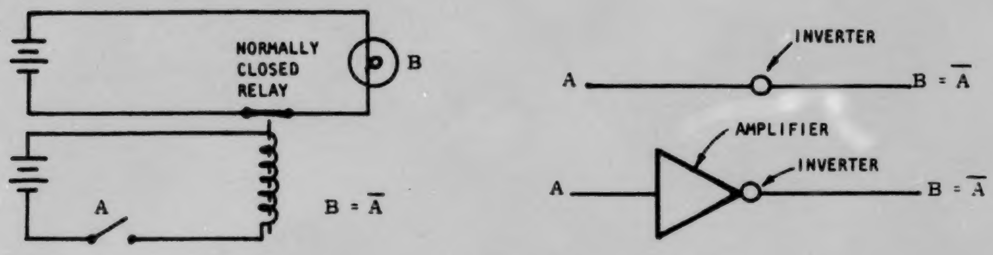
B. Logic diagram.

Fig 2-4. Combination OR-AND circuit.

Note: Parentheses are used to group related terms. For instance, the expression (A + B) (C + D) means, "AND" the quantity A + B with the quantity C + D.

d. The NOT function. A basic concept in Boolean algebra that has no counterpart in ordinary algebra is the NOT function which denotes the complement of the Boolean expression. A line over an expression is used in Boolean algebra to indicate the NOT function. Therefore, $\overline{0}$ means NOT 0, and has the same value as 1 because 1 is the only other value it can have. For the same reason, $\overline{1}$ has the value of 0. So, if A is 1, then $\overline{A}$ is 0; and when A is 0, $\overline{A}$ is 1. The NOT function may also be indicated by the prime sign ('). That is, $\overline{A}$ may also be written A'.

The basic NOT circuit is a single-input circuit (fig 2-5A) whose output is inverse of the input. That is, if switch A is closed, the relay will open the circuit to the light. The light will glow only when switch A is not closed. The logic symbol for the circuit is given in figure 2-5B. The upper diagram is used when a relay or other direct switching device is used. The lower diagram is used if amplification takes place at the same time as inversion, such as with a tube or transistor.

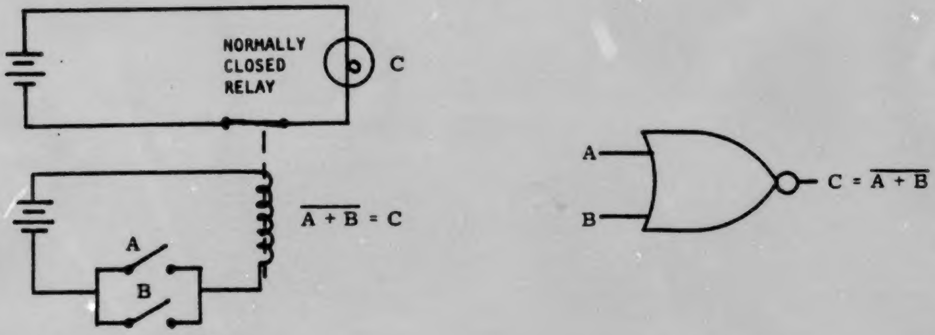

NORMALLY CLOSED RELAY
B
A
B = $\overline{A}$
INVERTER
A
B = $\overline{A}$
AMPLIFIER
INVERTER
A
B = $\overline{A}$

A. Simplified circuit.

B. Logic symbol.

Fig 2-5. NOT circuit.

e. The NOR and NAND functions. The NOT function is frequently combined with an OR or AND function. In figure 2-7A, the light will go out (NOT light up) when switch A or B is closed. The logic symbol for this circuit is shown in figure 2-6B.

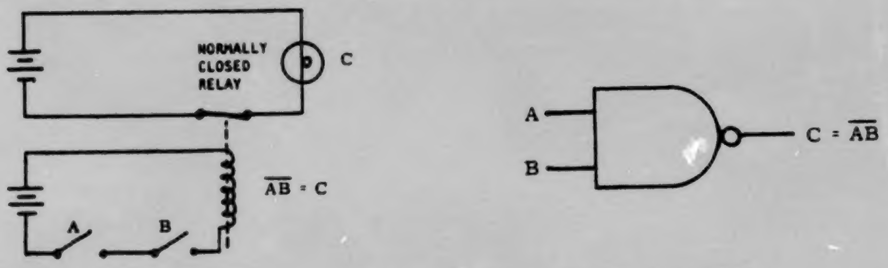

NORMALLY CLOSED RELAY
C
$\overline{A + B}$ = C
A
B
A
B
C = $\overline{A + B}$

A. Simplified circuit.

B. Logic symbol.

Fig 2-6. NOR circuit.

In figure 2-6A, the light will go out (NOT light up) when switch A AND B are closed. The logic symbol for this circuit is shown in figure 2-7B.


NORMALLY CLOSED RELAY
C
$\overline{AB}$ = C
A
B
A
B
C = $\overline{AB}$

A. Simplified circuit.

B. Logic symbol.

Fig 2-7. NAND circuit.

2-3. SIGNAL LEVELS

a. In the preceding discussion, we noted manually actuated switches which caused lights to go on or off in accordance with Boolean algebra functions. In actual application, such a function is performed by an input signal to the circuit, and the level of the signal determines whether the circuit will be activated or deactivated.

There are two rigidly controlled signal levels present in digital equipments which utilize binary circuits. These levels are referred to as HIGHS (most positive) and LOWS (least positive).

(1) HIGHS. A high-level signal normally represents the value one (1). Equipment designed to represent the presence of a Boolean expression with HIGHS is said to be using positive logic.

(2) LOWS. A low-level signal normally represents the value zero (0) or the absence of a Boolean expression. However, some applications do use LOWS to indicate the presence of Boolean expressions -- and the equipment is said to be using negative logic.

b. The particular signal level required at the input and present at the output of a logic circuit when it is activated (performing the indicated function) is indicated on the logic symbol by the presence or absence of a small circle (state indicator) (fig 2-8). If no circle is present at the output, the circuit is assumed to have a HIGH output when it is activated. The presence of a circle indicates a LOW level output of the circuit when it is activated. The presence of a state indicator at the input indicates that the output will be the NOT function of the Boolean expression at the point in question.

Of equal importance is the concept that the circuit will be inhibited (not activated) when a Boolean expression present at the input differs from that indicated on the diagram. Thus, if a $\overline{A}$ (NOT A) is indicated, the circuit will be activated by $\overline{A}$ and inhibited by A.

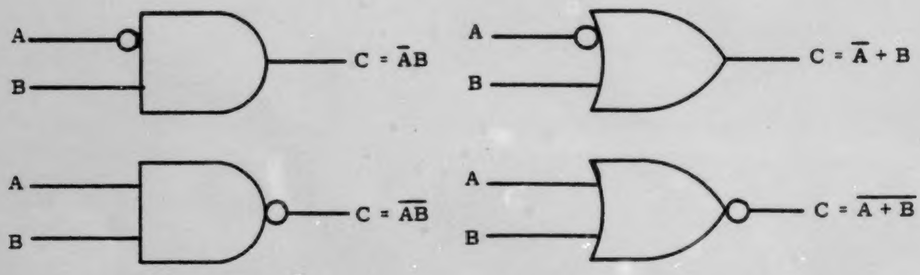


Fig 2-8. State indicators.

2-4. APPLICATION OF BOOLEAN ALGEBRA

The logical algebra developed by Boole has been extended and developed into several new fields of mathematics. However, this chapter covers Boolean algebra only to the extent necessary to understand the logical functions performed by digital circuits.

A short review of the basic logical functions of Boolean algebra and the logic symbols which have been developed to illustrate them will aid in understanding their application.

a. The OR function is performed by the OR gate (fig 2-1), which is activated when any of its required inputs is present. If no required input is present, the OR gate is inhibited.

b. The AND function is performed by the AND gate (fig 2-2), which is activated only when all of its required inputs are present. If any required input is absent, the AND gate is inhibited.

c. The NOT function is used to express the absence of an expression. If signal A is absent, then signal NOT A is present.

2-5. BOOLEAN EQUATION

The Boolean equation is a mathematical statement of logical functions, and it can be displayed pictorially by a logic diagram. Conversely, a Boolean equation can be written for any given logic diagram.

a. In writing the Boolean equation for a logic diagram, we note that the output of a gate or series of gates is composed of the individual inputs necessary to activate the gate or gates. We begin the equation by writing the output for the input gate or gates. Then, step by step we write an output for each gate, proceeding toward the final (output) gate. For example, in figure 2-9A we first wrote an expression for the output of gate 1. This output, A · B, is shown (fig 2-9A) as an input to gate 2, along with input C. The output from gate 1 is a spoken of as being OR'ed with input C in gate 2. Then output L will be present when A AND B are present OR when C is present. This is written AB + C = L.

Figure 2-9B shows the output of an OR gate being used as an input to an AND gate. The output of gate 1, which is A + B, is shown in figure 2-9B as an input to gate 2, along with input C. The output from gate 1 is spoken of as being AND'ed with input C in gate 2. Then output L will be present when A OR B is present AND C is present. This is written (A + B) C = L.

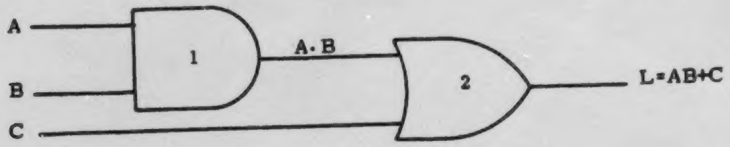


Fig 2-9A.

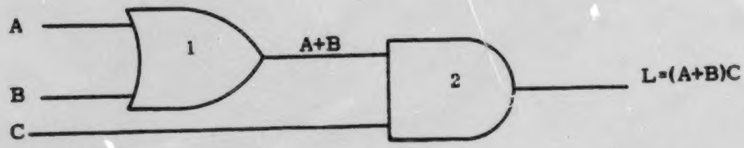


Fig 2-9B.

Fig 2-9. Logic diagram.

Figure 2-10 illustrates how the NOT function of an expression may be used as an input. The state indicator, which appears at the input of the AND gate, does not necessarily illustrate a physical component, but rather that the input circuit is constructed so that logical inversion occurs. In figure 2-10, gate 1 will be activated when the expressions A AND B are present as inputs. (The inversion from B to $\overline{B}$ takes place within the gate.)

When gate 1 of figure 2-10 is activated, the output is $A\overline{B}$. The inputs required to activate gate 2 are the output of gate 1 OR C; therefore, the output of gate 2 is $C + A\overline{B}$. The inputs required to activate gate 3 are the outputs of gates 2 AND D AND E; therefore, the output of gate 3 is $L = E\overline{D}(C + A\overline{B})$.

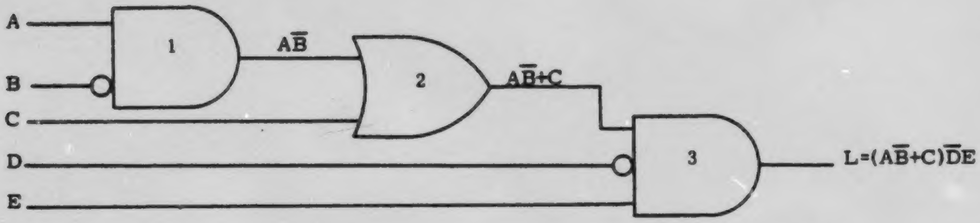

A
B
C
D
E
1
$A\overline{B}$
2
$A\overline{B}+C$
3
$L=(A\overline{B}+C)\overline{D}E$

Fig 2-10. Logic diagram.

Figure 2-11 illustrates how the NOT function output from a gate can be used logically as an input to a following gate. In figure 2-11, the state indicator at the output of gate 1 indicates that when A AND B are present at the input, the gate will be activated and the output will be AB.

For gate 2 of figure 2-11 to be activated, C must be present or the NOT function expression from gate 1 must be present. Thus the output expression for gate 2 is C + (AB) = L.

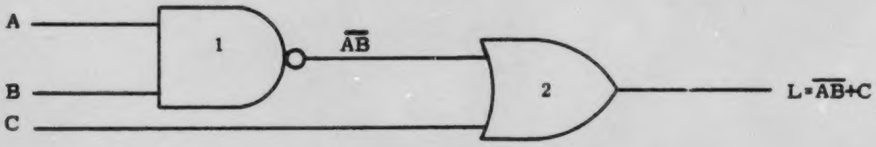

A
B
C
1
$\overline{AB}$
2
$L=\overline{AB}+C$

Fig 2-11. Logic diagram.

2-6. DRAWING LOGIC DIAGRAMS

In drawing logic diagrams for a Boolean expression, the object is to draw the gates and functions necessary to generate the expression from individual signal terms. The steps to be observed are as follows:

a. The individual terms of the expression are used as inputs to the gates.

b. The sign of operation between terms indicates the type of logic gate required.

c. The NOT function indicates that logical inversion is required.

Examples: The first gate to be drawn for the expression $F + \left[E\overline{D}\,(A\overline{B} + C)\right]$ is the OR gate shown in figure 2-12.

The OR gate input $E\overline{D}\,(A\overline{B} + C)$ shown in figure 2-12 is the output of the 3-input AND gate shown in figure 2-13.

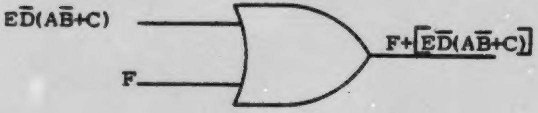

$E\overline{D}(A\overline{B}+C)$
F
$F+[E\overline{D}(A\overline{B}+C)]$

Fig 2-12. Logic diagram.

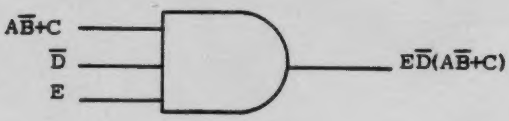

$A\overline{B}+C$
$\overline{D}$
E
$E\overline{D}(A\overline{B}+C)$

Fig 2-13. Logic diagram.

The AND gate input $A\overline{B} + C$ shown in figure 2-13 is the output of the 2-input OR gate shown in figure 2-14.

The OR gate input $A\overline{B}$ shown in figure 2-14 is the output of the 2-input OR gate shown in figure 2-15.

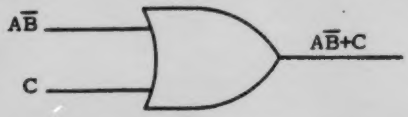


Fig 2-14. Logic diagram.

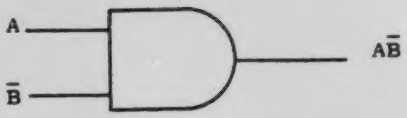


Fig 2-15. Logic diagram.

The complete logic diagram is shown in figure 2-16. Notice that the state indicator symbol has been added to inputs B and D of gates 1 and 3, respectively, indicating that logical inversion occurs.

Note: To check a Boolean expression, reverse the diagraming procedure. Starting with the inputs, determine whether the outputs of successive gates, including the final output, are correctly expressed.

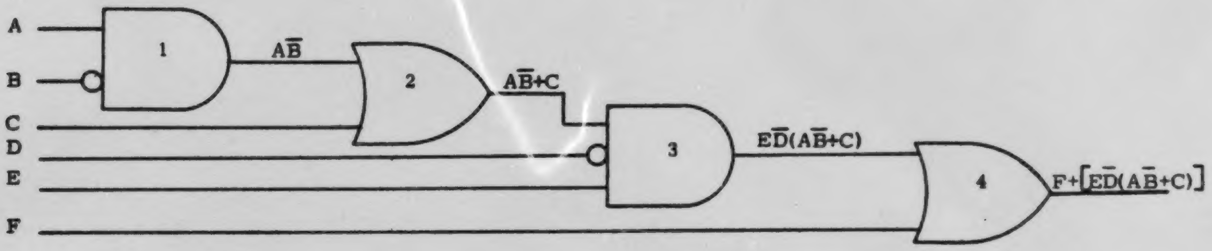

A
B
C
D
E
F
1
$A\overline{B}$
2
$A\overline{B}$+C
3
$E\overline{D}(A\overline{B}+C)$
4
$F+[E\overline{D}(A\overline{B}+C)]$

Fig 2-16. Logic diagram.

2-7. THEOREMS AND TRUTH TABLES

As previously pointed out, Boolean algebra is a valuable aid in the design and analysis of switching circuits. For instance, it is easier to calculate with mathematical expressions that represent switching circuits than to analyze schematic or logic diagrams. In addition, once the logic diagrams have been drawn, Boolean algebra provides a straightforward way of describing the circuitry used.

The fundamental concepts upon which Boolean algebra is based have been presented and described with simplified circuits and logic diagrams. We now discuss those Boolean algebra theorems which state most of the basic rules by which Boolean expressions may be simplified. These theorems and their names are shown in figure 2-17.

In studying a Boolean expression, it is helpful to construct a tabulation (called a truth table) and use it to evaluate each combination of variables in the expression, and to prove that a Boolean equation is true or to show its falseness. In other words, the truth table enables you to compare the right side of a Boolean equation with the left side, to see if they are equivalent in value. This method of proof is called proof by perfect induction.

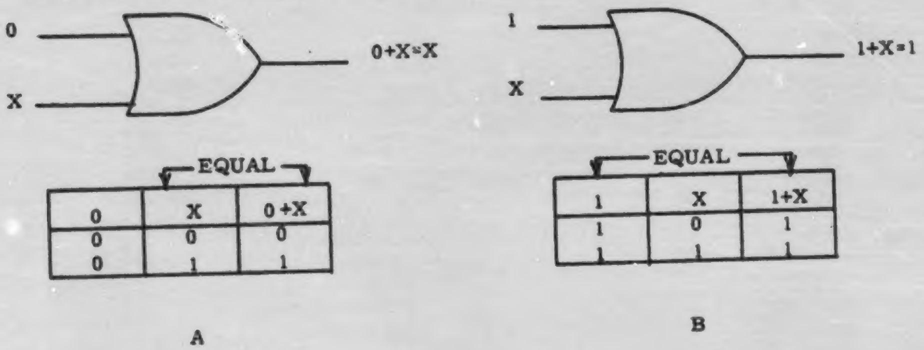
Union	$0 + X = X$ $1 + X = 1$
Intersection	$0 \cdot X = 0$ $1 \cdot X = X$
Idempotent	$X + X = X$ $X \cdot X = X$
Complementary	$X + \overline{X} = 1$ $X \cdot \overline{X} = 0$
Double negative	$\overline{\overline{X}} = X$
Commutative	$X + Y = Y + X$ $X \cdot Y = Y \cdot X$
Associative	$X + (Y+Z) = (X+Y) + Z$ $X(YZ) = (XY)Z$
Distributive	$XY + XZ = X(Y+Z)$ $(X+Y)(X+Z) = X + YZ$ $WY+WZ+XY+XZ = (W+X)(Y+Z)$
Absorption	$X + XY = X$ $X(X+Y) = X$
DeMorgan's	$\overline{XYZ} = \overline{X} + \overline{Y} + \overline{Z}$ $\overline{X + Y + Z} = \overline{X} \cdot \overline{Y} \cdot \overline{Z}$
Common Identities	$X+\overline{X}Y = X+Y$ $X(\overline{X}+Y) = XY$

Fig 2-17. Boolean algebra theorems.

a. Union theorems. These expressions indicate logical addition (the OR function). They are simple in that there is only one variable, and it can assume only the value of 0 or 1.

(1) $0 + X = X$ means that the logical addition of 0 to an expression does not affect the result (fig 2-18A). The truth table proves that for each value of the variable X, the expression $0 + X$ is equal to the variable. In other words, 0 input to an OR gate has no effect on the output.

(2) 1 + X = 1 means that the logical addition of 1 to an expression results in a value of 1 (fig 2-18B). The truth table proves that the value of the variable X does not affect the result. That is, if any input to an OR gate is 1, the output is 1.



0	X	0+X
0	0	0
0	1	1

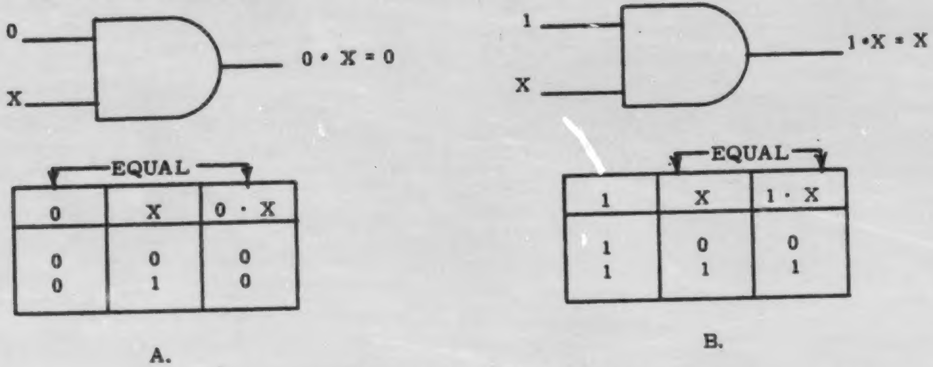
1	X	1+X
1	0	1
1	1	1

Fig 2-18. Logic diagrams for union theorems.

b. Intersection theorems. These expressions indicate logical multiplication (the AND function) involving only one variable.

(1) 0 · X = 0 means that the logical multiplication of an expression by 0 results in a value of 0 (fig 2-19A). In other words, if any input to an AND gate is 0, the output is 0.

(2) 1 · X = X means that the logical multiplication of an expression by 1 does not affect the result (fig 2-19B). When the inputs to an AND gate are 1 and a variable, the output is equal to the variable.



0	X	0 · X
0	0	0
0	1	0

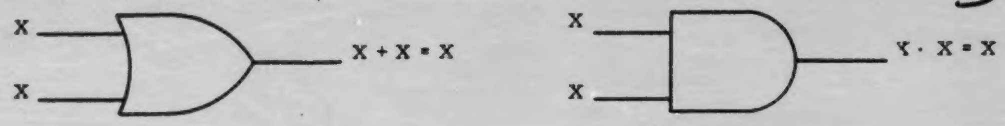
1	X	1 · X
1	0	0
1	1	1

Fig 2-19. Logic diagrams for intersection theorems.

c. Idempotent theorems.

(1) X + X = X means that the logical addition of an expression to itself results in the expression (fig 2-20A). That is, if the inputs to an OR gate are identical, the output is identical.

(2) X · X = X means that the logical multiplication of an expression by itself results in the expression (fig 2-20B). Or, if the inputs to an AND gate are identical, the output is identical.



A.

EQUAL

X	$X + X$
0	0
1	1

B.

EQUAL

X	$X \cdot X$
0	0
1	1

Fig 2-20. Logic diagrams for idempotent theorems.

d. Complementary theorems.

(1) $X + \bar{X} = 1$ means that the logical addition of an expression and its complement results in a value of 1 (fig 2-21A). In other words, if an input and its complement are OR'ed, the output is 1.

(2) $X \cdot \bar{X} = 0$ means that the logical multiplication of an expression and its complement results in a value of 0 (fig 2-21B). When an input and its complement are AND'ed,the output is 0.

X
X̄
X + X̄ = 1
X
X̄
X · X̄ = 0

A.

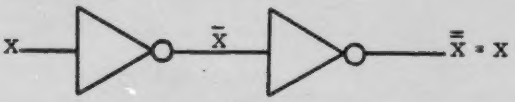
X	$\bar{X}$	$X + \bar{X} =$
0	1	1
1	0	1

B.

X	$\bar{X}$	$X \quad \bar{X}$
0	1	0
1	0	0

Fig 2-21. Logic diagrams for complementary theorems.

e. Double-negative theorem. $\bar{\bar{X}} = X$ means that a double inversion of an expression results in the original expression (fig 2-22). If a signal is sent through two inverter stages, the output is equivalent to the original signal.



EQUAL

X	$\bar{X}$	$\bar{\bar{X}}$
0	1	0
1	0	1

Fig 2-22. Logic diagram for double-negative theorem.

f. Commutative theorems. These expressions indicate that the sequence of terms has no effect on the value of the expression. The output terms of an AND or an OR gate may be written in any order without affecting the value.

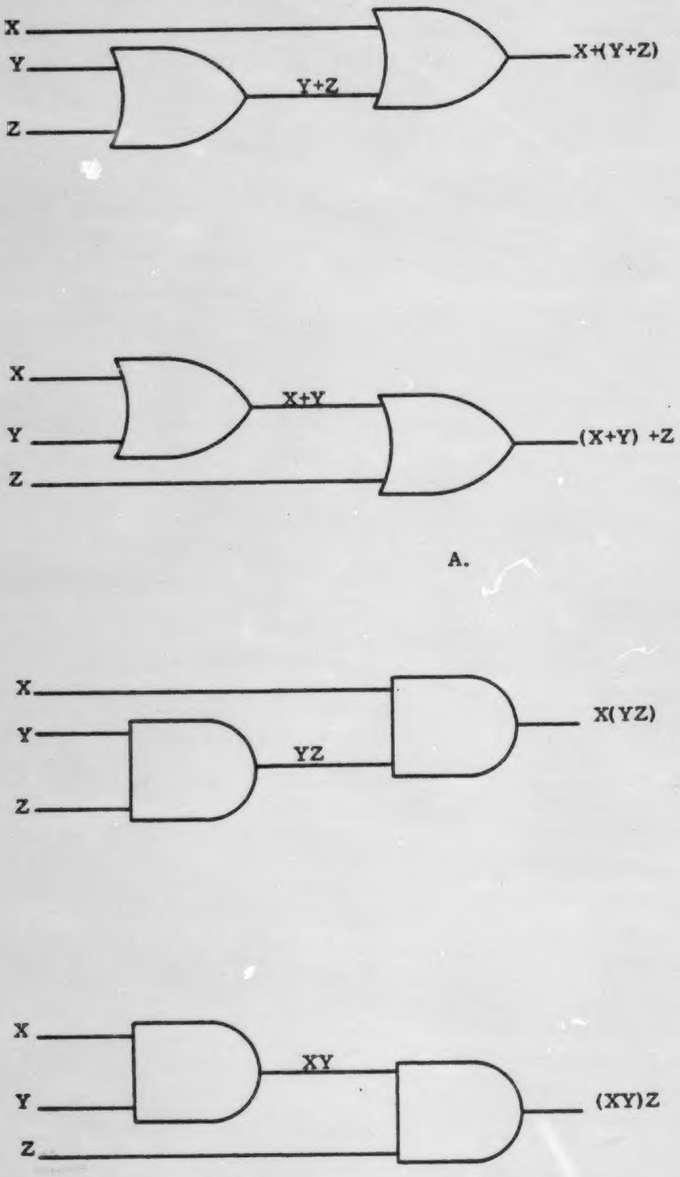
(1) $X + Y = Y + X$.

(2) $X \cdot Y = Y \cdot X$.

g. Associative theorems. These expressions indicate that the grouping of terms has no effect on the value of the expressions.

(1) X + (Y + Z) = (X + Y) + Z. The output terms of a series of OR gates may be grouped in any order without affecting the value (fig 2-23A).

(2) X(YZ) = (XY)Z. The output terms of a series of AND gates may be grouped in any order without affecting the value (fig 2-23B).



X	Y	Z	Y+Z	X+(Y+Z)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

EQUAL

X	Y	Z	X+Y	(X+Y)+Z
0	0	0	0	0
0	0	1	0	1
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

X	Y	Z	Y· Z	X(YZ)
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

EQUAL

X	Y	Z	X· Y	(XY)Z
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	1	0
1	1	1	1	1

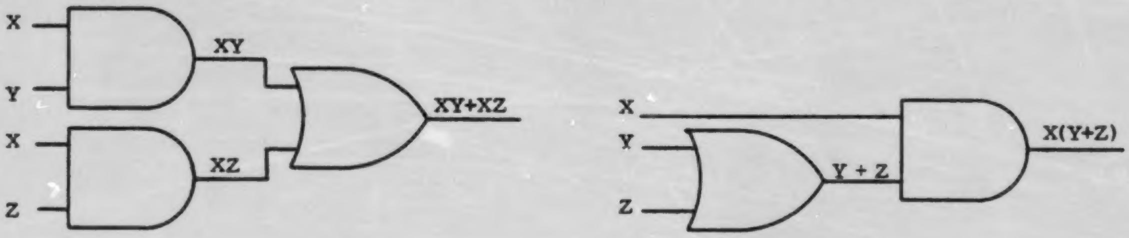
Fig 2-23. Logic diagrams for associative theorems.

h. Distributive theorems. These expressions indicate logical addition or multiplication where one variable appears in each of the terms.

(1) XY + XZ = X(Y + Z). Indicates a logical addition of products containing an expression in common (fig 2-24A). AND'ing an expression with each input of an OR gate is equivalent to AND'ing the expression with the output of the OR gate.

(2) (X + Y)(X + Z) = X + YZ indicates a logical multiplication of sums containing an expression in common (fig 2-24B). OR'ing an expression with each input of an AND gate is equivalent to OR'ing the expression to the output of the AND gate.

(3) WY + WZ + XY + XZ = (W+X) (Y+Z) indicates a logical addition of products containing an expression in common (fig 2-24C). OR'ing an expression with each output of an AND gate is equivalent to AND'ing the expression to the outputs of the OR gates.

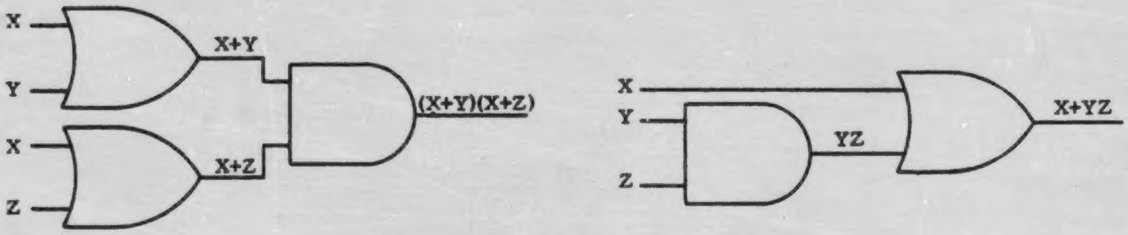


EQUAL

X	Y	Z	XY	XZ	XY+XZ
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	1	1

X	Y	Z	Y+Z	X(Y+Z)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

A.

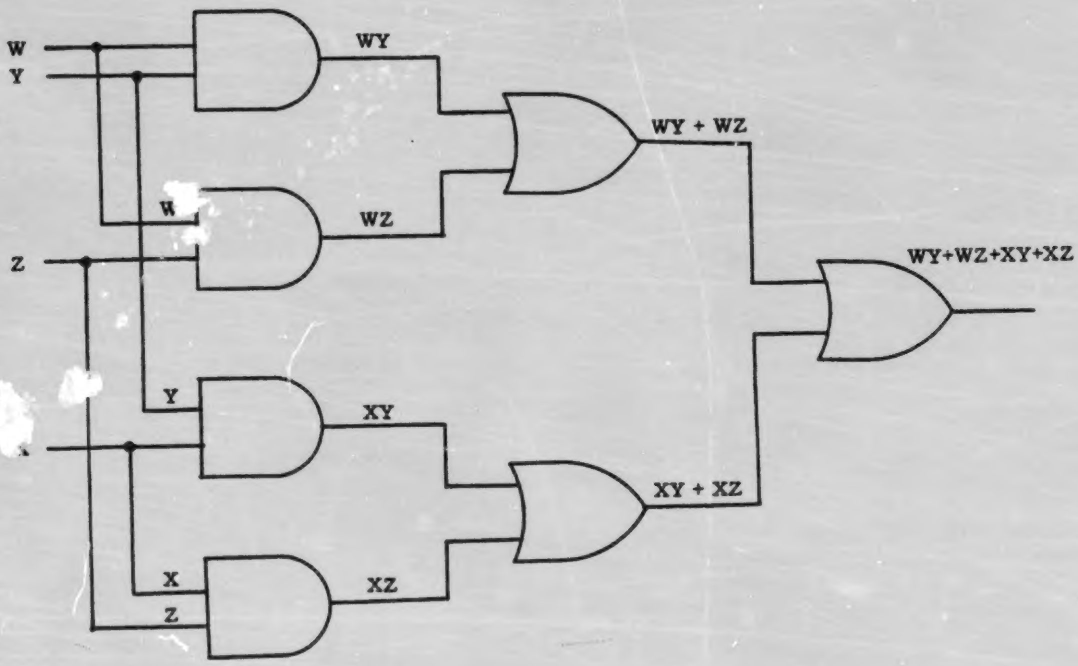


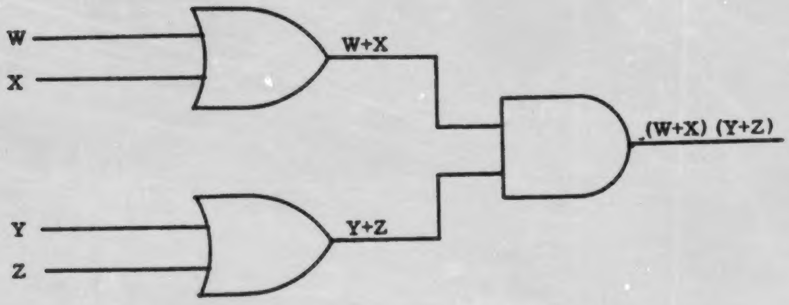
EQUAL

X	Y	Z	X+Y	X+Z	(X+Y)(Y+Z)
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	1	1
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	1	1	1

X	Y	Z	YZ	X+YZ
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

B.


W
Y
WY
WY + WZ
W
WZ
Z
WY+WZ+XY+XZ
Y
XY
XY + XZ
X
Z
XZ


W
X
W+X
(W+X) (Y+Z)
Y
Z
Y+Z

EQUAL

WY	WZ	XY	XZ	WY+WZ	XY+XZ	WY+WZ+XY+XZ
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0
0	0	0	1	0	1	1
0	0	1	0	0	1	1
0	0	1	1	0	1	1
0	0	0	0	0	0	0
0	1	0	0	1	0	1
1	0	0	0	1	0	1
1	1	0	0	1	0	1
0	0	0	0	0	0	0
0	1	0	1	1	1	1
1	0	1	0	1	1	1
1	1	1	1	1	1	1

W	X	Y	Z	W+X	Y+Z	(W+X) (Y+Z)
0	0	0	0	0	0	0
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	1	1	1
0	1	1	0	1	1	1
0	1	1	1	1	1	1
1	0	0	0	1	0	0
1	0	0	1	1	1	1
1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	1	0	0	1	0	0
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

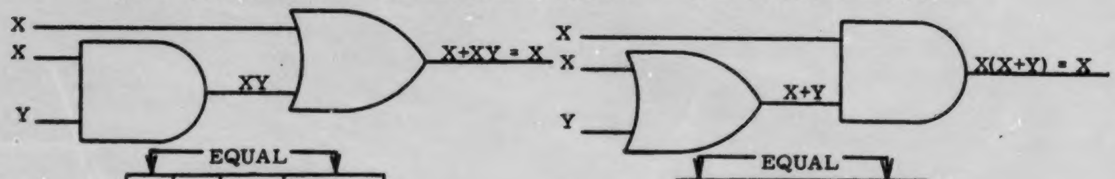
C.

Fig 2-24--contd

i. **Absorption theorems.** These expressions indicate the logical addition or multiplication of a variable with terms containing that variable.

(1) $X + XY = X$ means that the logical addition of an expression and a product containing that expression results in the original expression (fig 2-25A). If the output of an AND gate is OR'ed with one of the AND gate's inputs, the result is equal to that input.

(2) $X(X + Y) = X$ means that the logical multiplication of an expression and a sum containing that expression results in the original expression (fig 2-25B). If the output of an OR gate is AND'ed with one of the OR gate's inputs, the result is equal to that input.


X
X
Y
XY
X+XY = X
EQUAL
X
X
Y
X+Y
X(X+Y) = X
EQUAL

X	Y	XY	X+XY
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	1

A.

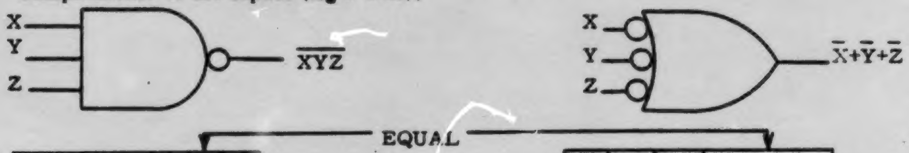
X	Y	X+Y	X(X+Y)
0	0	0	0
0	1	1	0
1	0	1	1
1	1	1	1

B.

Fig 2-25. Logic diagrams for absorption theorems.

j. **DeMorgan's theorem.** . These expressions indicate that the complement of an expression is the equivalent of the complement of the individual terms with the connecting signs changed.

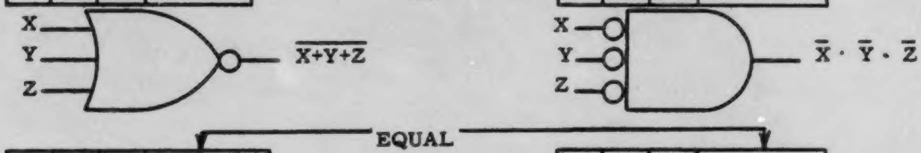
(1) $\overline{XYZ} = \overline{X} + \overline{Y} + \overline{Z}$. Complementing the output of an AND gate is equivalent to OR'ing the complements of the inputs (fig 2-26A).


X
Y
Z
$\overline{XYZ}$
X
Y
Z
$\overline{X}+\overline{Y}+\overline{Z}$
EQUAL

X	Y	Z	$\overline{XYZ}$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

A.

X	Y	Z	$\overline{X}+\overline{Y}+\overline{Z}$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0


X
Y
Z
$\overline{X+Y+Z}$
X
Y
Z
$\overline{X} \cdot \overline{Y} \cdot \overline{Z}$
EQUAL

X	Y	Z	$\overline{X+Y+Z}$
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

B.

X	Y	Z	$\overline{X} \cdot \overline{Y} \cdot \overline{Z}$
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

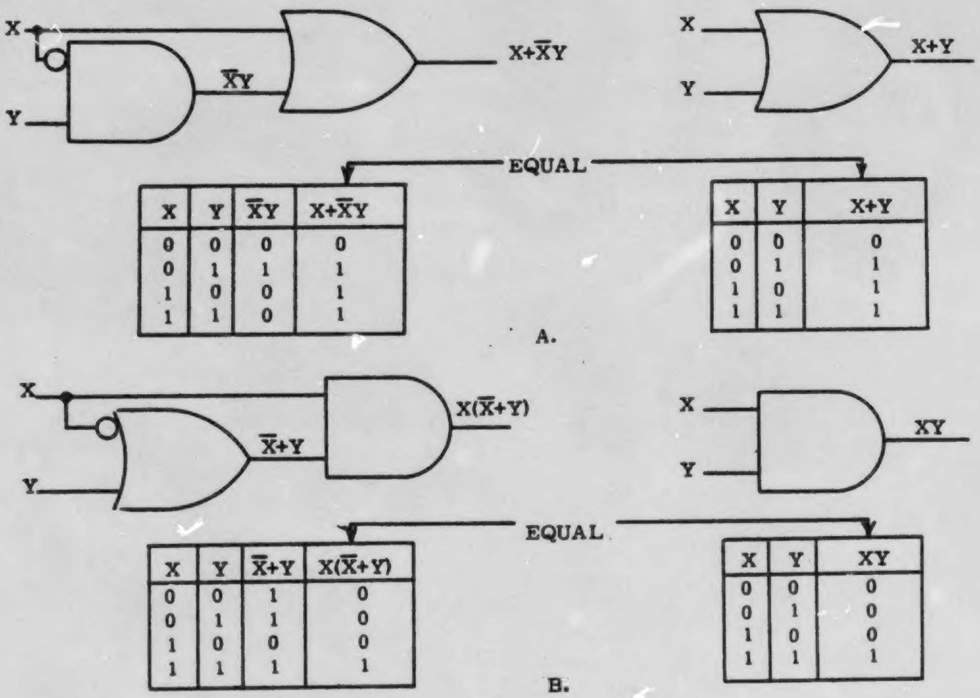
Fig 2-26. Logic diagrams for DeMorgan's theorems.

(2) $\overline{X + Y + Z} = \overline{X} \cdot \overline{Y} \cdot \overline{Z}$. Complementing the output of an OR gate is equivalent to AND'ing the complements of the inputs (fig 2-26B).

k. Common identities. These expressions indicate the logical addition or multiplication of a variable with terms containing the complement of that variable.

(1) $X + \overline{X}Y = X + Y$ means that the logical addition of a variable (X) by the product of an expression (Y) and the complement of the variable ($\overline{X}$) results in the logical sum of the variable and the expression (fig 2-27A). In other words, AND'ing the complement of one input to an OR gate with another input of the OR gate has no effect on its output.

(2) $X(\overline{X} + Y) = XY$ means that the logical multiplication of a variable (X) to the sum of an expression (Y) and the complement of the variable ($\overline{X}$) results in the logical product of the variable and the expression (fig 2-26B). In other words, OR'ing the complement of one input to an AND gate with another input of the AND gate has no effect on its output.



X	Y	$\overline{X}Y$	$X+\overline{X}Y$
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	1

X	Y	X+Y
0	0	0
0	1	1
1	0	1
1	1	1

A.

X	Y	$\overline{X}+Y$	$X(\overline{X}+Y)$
0	0	1	0
0	1	1	0
1	0	0	0
1	1	1	1

X	Y	XY
0	0	0
0	1	0
1	0	0
1	1	1

B.

Fig 2-27. Logic diagrams for the common identities.

2-8. SIMPLIFYING BOOLEAN EQUATIONS

It has been shown that a logical configuration which has been designed to produce a certain output can sometimes be replaced by a simplified logic circuit which is equivalent, and it will produce the same output.

a. Let us assume that we need a circuit which will provide an output X with any of the following inputs: A and C, A and D, B and C, or B and D. Thus, the Boolean equation is:

$$X = AC + AD + BC + BD$$

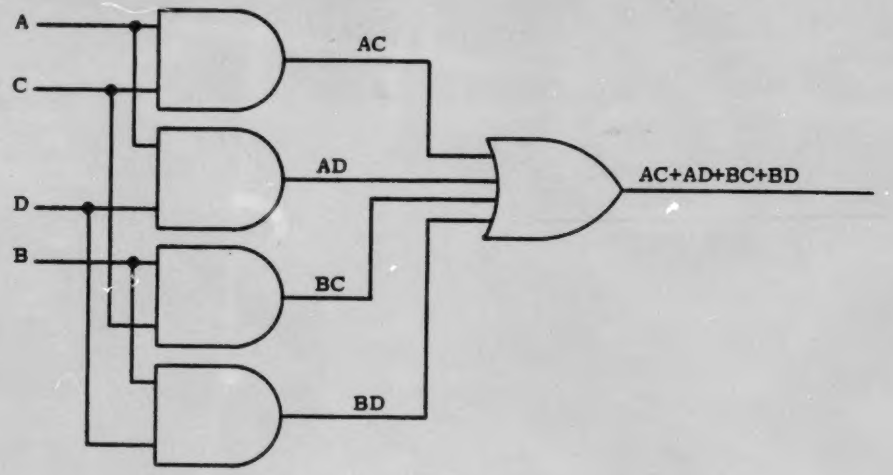


Fig 2-28. Logic diagram.

The logic diagram for this equation is shown in figure 2-28. We see that we have 12 signal paths with associated gate circuitry. We shall now see how Boolean algebra can be used to indicate a simplified circuit. Apply the distributive theorem AC + AD = A(C + D) and BC + BD = B(C + D). Substituting these values in the original equation gives X = A(C + D) + B(C + D).

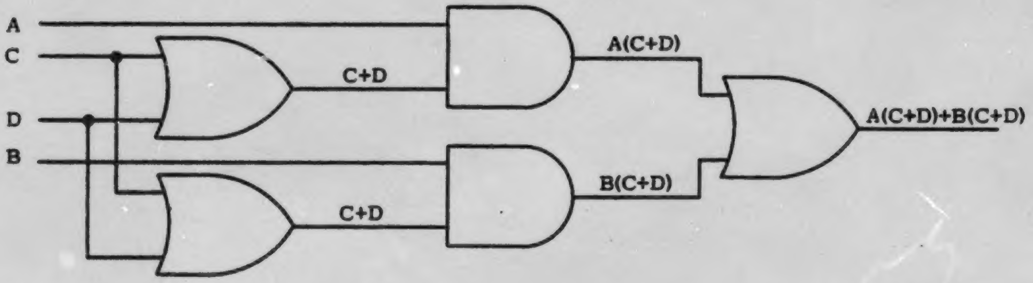


Fig 2-29. Logic diagram.

The circuit will now appear as shown in figure 2-29. Now only 10 signal paths are needed to perform the same job as the original 12. We are not finished with the job of simplification, however. Since the factor C + D appears twice, we can apply the distributive theorem again and the equation becomes X = (A + B) (C + D). Only 6 signal paths and 3 gates are needed for this circuit (fig 2-30). -- Here we should check the original requirements and ask ourselves, will this simplified circuit perform the required operations?

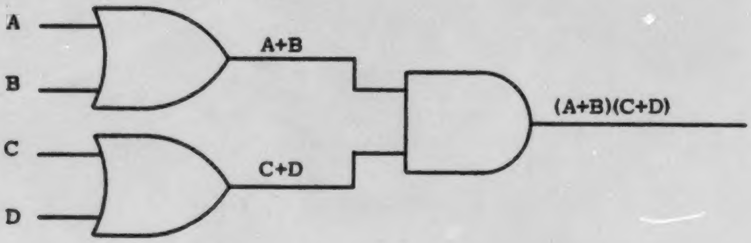


Fig 2-30. Logic diagram.

Exercise: Simplify:

$$(A + B)(B + C) + (\overline{A + B})(\overline{B + C})$$

$$(\overline{C}DF + A + D + AD\overline{A})(A + BD + EA + D)$$

(Check your answers with those on page 2-21.)

b. Another circuit is required which will provide an output X when the 3-digit binary input represents a prime number (e.g., decimal 2, 3, 5, 7). Assigning the letters A, B, C to the place positions, we have:

Decimal	Binary	Boolean
2	010	$\overline{A}B\overline{C}$
3	011	$\overline{A}BC$
5	101	$A\overline{B}C$
7	111	ABC

And the Boolean equation is the logical sum of these products: $X = \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}C + ABC$.

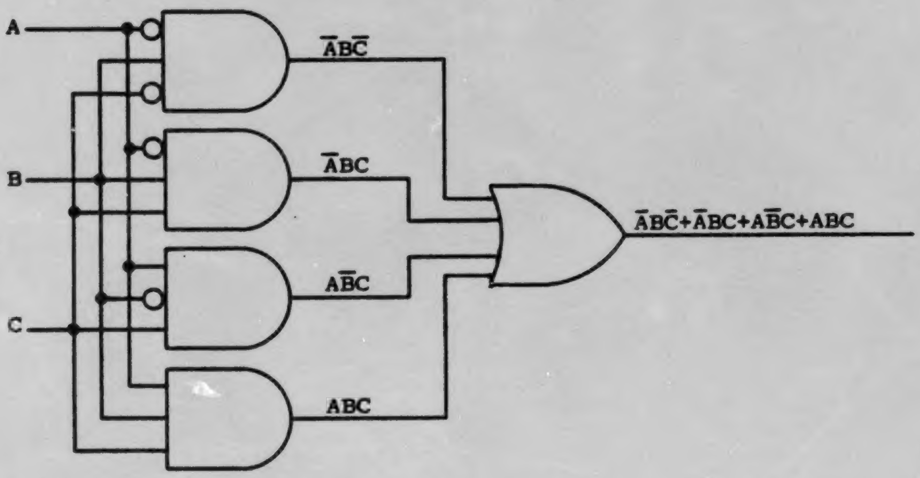

A
B
C
$\overline{A}B\overline{C}$
$\overline{A}BC$
$A\overline{B}C$
ABC
$\overline{A}B\overline{C}+\overline{A}BC+A\overline{B}C+ABC$

Fig 2-31. Logic diagram.

The logic diagram for this equation (fig 2-31) shows 5 gates with 16 signal paths. We can simplify this equation by applying the indicated theorems:

	$X = \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}C + ABC$
Commutative	$= \overline{C}\overline{A}B + C\overline{A}B + \overline{B}AC + BAC$
Associative	$= \overline{C}(\overline{A}B) + C(\overline{A}B) + \overline{B}(AC) + B(AC)$
Distributive	$= (\overline{C} + C)(\overline{A}B) + (\overline{B} + B)(AC)$
Complementary	$= (1)(\overline{A}B) + (1)(AC)$
Intersection	$= \overline{A}B + AC$

The logic diagram for this equation (fig 2-32) requires only 3 gates and 6 signal paths. The table below shows the expression to be correct.

Decimal	ABC	$\bar{A}B$	AC	$\bar{A}B + AC$
0	000	0	0	0
1	001	0	0	0
2	010	1	0	1
3	011	1	0	1
4	100	0	0	0
5	101	0	1	1
6	110	0	0	0
7	111	0	1	1

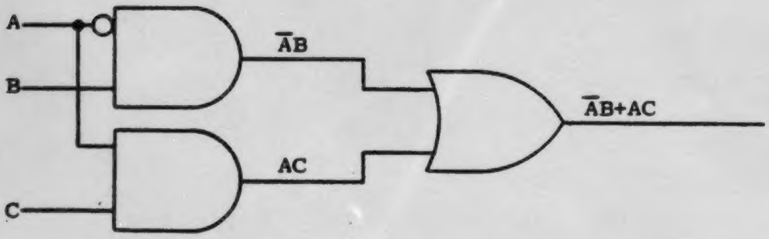


Fig 2-32. Logic diagram.

Exercise: The table below represents a binary addition where A and B are the two digits to be added and C is the carry digit from the next lower place position.

ABC	X	Y
000	0	0
001	1	0
010	1	0
011	0	1
100	1	0
101	0	1
110	0	1
111	1	1

Write and simplify the Boolean equation for the sum digit X and then the carry to the next higher place-position Y. (Check your answers with those on page 2-22.)

c. Boolean algebra can also be used to devise circuits that, though not always the simplest, use only one type of gate throughout. NOR gates are commonly used in this manner. Knowing the desired output, we determine the inputs necessary to produce it. If the desired output of the final NOR gate (fig 2-33) is the same as that of figure 2-32, the signal before the final inversion is the complement of the output or: $\overline{\bar{A}B + AC}$

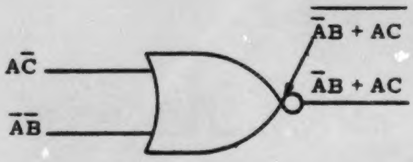


Fig 2-33. Logic diagram.

To obtain the inputs, it is necessary to simplify the expression:

$$X = \overline{\bar{A}B + AC}$$

	$X = \overline{\bar{A}B + AC}$
DeMorgan's	$= (\overline{\bar{A}B})\ (\overline{AC})$
DeMorgan's	$= (\bar{\bar{A}} + \bar{B})\ (\bar{A} + \bar{C})$
Double negative	$= (A + \bar{B})\ (\bar{A} + \bar{C})$
Distributive	$= A(\bar{A} + \bar{C}) + \bar{B}(\bar{A} + \bar{C})$
Distributive	$= A\bar{A} + A\bar{C} + \bar{B}\bar{A} + \bar{B}\bar{C}$
Complementary	$= 0 + A\bar{C} + \bar{B}\bar{A} + \bar{B}\bar{C}$
Union	$= A\bar{C} + \bar{B}\bar{A} + \bar{B}\bar{C}$
Complementary	$= A\bar{C} + \bar{B}\bar{A} + (A + \bar{A})\bar{B}\bar{C}$
Distributive	$= A\bar{C} + \bar{B}\bar{A} + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C}$
Commutative	$= A\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B} + \bar{A}\bar{B}\bar{C}$
Absorption	$= A\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}$
Absorption	$= A\bar{C} + \bar{A}\bar{B}$

These are the two inputs of the final NOR gate (fig 2-33), each being the output of another NOR gate (fig 2-34). Their inputs are determined in the same manner:

	$\overline{A\bar{C}}$	$\overline{\bar{A}\bar{B}}$
DeMorgan's	$\bar{A} + \bar{\bar{C}}$	$\bar{\bar{A}} + \bar{\bar{B}}$
Double negative	$\bar{A} + C$	$A + B$

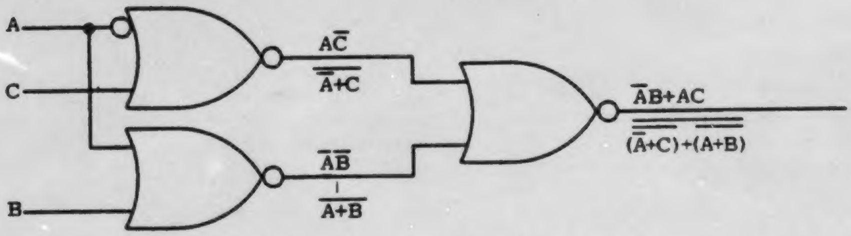


Fig 2-34. Logic diagram.

By writing the Boolean equation for the diagram (fig 2-34), using these inputs and simplifying, we should obtain the original output expression:

	$X = \overline{\overline{(\bar{A} + C)} + \overline{(A + B)}}$
DeMorgan's	$= \bar{\bar{(\bar{A} + C)}}\ \bar{\bar{(A + B)}}$
Double negative	$= (\bar{A} + C)\ (A + B)$
Distributive	$= \bar{A}(A + B) + C(A + B)$
Distributive	$= \bar{A}A + \bar{A}B + CA + CB$
Complementary	$= \bar{A}B + CA + CB$
Complementary	$= \bar{A}B + CA + (A + \bar{A})CB$
Distributive	$= \bar{A}B + CA + ACB + \bar{A}CB$
Commutative	$= \bar{A}B + \bar{A}BC + AC + ACB$
Absorption	$= \bar{A}B + AC$

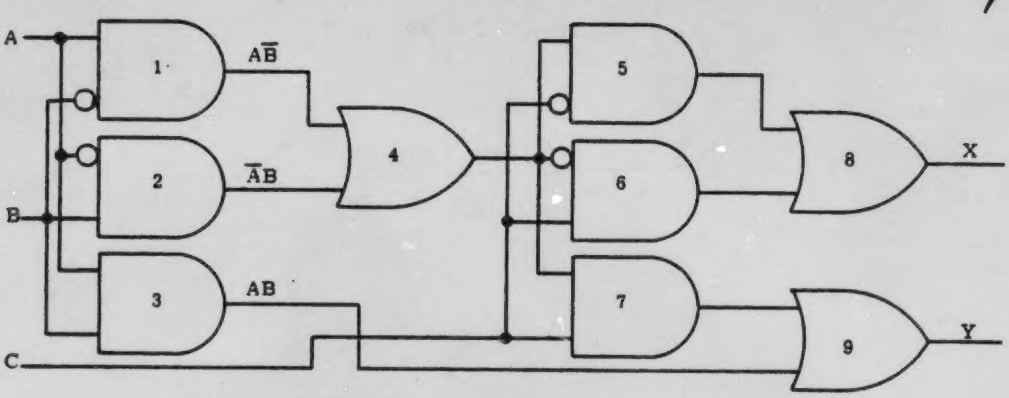


Fig 2-35. Circuit often used for binary addition.

Exercise: The outputs of gates 1, 2, and 3 are indicated. Write the output of each of the remaining gates. Simplify the expressions for X and Y. Are they the same as in the previous exercise? (Check your answers with those on page 2-22.)

2-9. SUMMARY

a. Boolean algebra is used to indicate the logic circuits needed to perform the logical functions of digital computers and other automatic switching networks. The three basic functions of Boolean algebra are the AND function, the OR function, and the NOT function. The AND gate, which performs the AND function, is activated only when all indicated inputs are present; if any is absent, the gate will be inhibited. The OR gate, which performs the OR function, will be activated when any of the indicated inputs is present; if all inputs are absent, the gate will be inhibited. The NOT function is used to express the inversion or complementation of a term. If signal A is absent, then NOT A is present.

b. The concept of equivalent expressions is used to simplify Boolean expressions and to indicate alternate circuits. The Boolean expression is a mathematical statement of logical functions, and it can be displayed pictorially by a logic diagram. To draw the logic diagram indicated by a Boolean expression, draw the gates indicated by the signs of operation, using the terms adjacent to each sign as inputs to the associated gate and observing logical inversion as indicated by occurrence of the NOT sign. Conversely, to write the Boolean expression indicated by a logic diagram, begin by writing the output for the input gate or gates. Then, step by step write an output for each gate, proceeding toward the final gate. An expression for any switching network, no matter how complex, can be written with this method.

ANSWERS TO EXERCISES

Exercise following para 2-8a:

Given:	$(A + B)(B + C) + (\overline{A + B})(\overline{B + C})$
Distributive	$AC + B + (\overline{A + B})(\overline{B + C})$
DeMorgan's	$AC + B + (\overline{A}\overline{B})(\overline{B}\overline{C})$
Idempotent	$AC + B + \overline{A}\overline{B}\overline{C}$
Common identity	$AC + B + \overline{A}\overline{C}$

Given:	$(\bar{C}DF + A + D + AD\bar{A})(A + BD + EA + D)$
Commutative	$\left[(A + AD\bar{A}) + (D + D\bar{C}F)\right]\left[(A + AE) + (D + DB)\right]$
Absorption	$(A + D)(A + D)$
Idempotent	$A + D$

Exercise following para 2-8b:

	$X = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$
Distributive	$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$
or	$= \bar{B}(\bar{A}C + A\bar{C}) + B(\bar{A}\bar{C} + AC)$
or	$= \bar{C}(\bar{A}B + A\bar{B}) + C(\bar{A}\bar{B} + AB)$
	$Y = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$
Idempotent	$= \bar{A}BC + ABC + A\bar{B}C + ABC + AB\bar{C} + ABC$
Distributive	$= BC(\bar{A} + A) + AC(\bar{B} + B) + AB(\bar{C} + C)$
Complementary	$= BC(1) + AC(1) + AB(1)$
Intersection	$= BC + AC + AB$

Exercise following para 2-8c:

Gate 4	$= A\bar{B} + \bar{A}B$
Gate 5	$= \bar{C}(A\bar{B} + \bar{A}B)$
Gate 6	$= C\overline{(A\bar{B} + \bar{A}B)}$
Gate 7	$= C(A\bar{B} + \bar{A}B)$
Gate 8	$X = \bar{C}(A\bar{B} + \bar{A}B) + C\,\overline{(A\bar{B} + \bar{A}B)}$
DeMorgan's	$= \bar{C}(A\bar{B} + \bar{A}B) + C\left[(\bar{A} + B)(A + \bar{B}\right]$
Distributive	$= \bar{C}(A\bar{B} + \bar{A}B) + C\left[\bar{A}(A + \bar{B}) + B(A + \bar{B})\right]$
Common identity	$= \bar{C}(A\bar{B} + \bar{A}B) + C\left[\bar{A}\bar{B} + AB\right]$
Gate 9	$Y = AB + C(A\bar{B} + \bar{A}B)$
Distributive	$= AB + A\bar{B}C + \bar{A}BC$
Idempotent	$= AB + A\bar{B}C + AB + \bar{A}BC$
Distributive	$= A(B + \bar{B}C) + B(A + \bar{A}C)$
Common identity	$= A(B + C) + B(A + C)$
Distributive	$= AB + AC + AB + BC$
Idempotent	$= AB + AC + BC$

Yes, X and Y are the same.

Chapter 3

LOGIC GATES

3-1. INTRODUCTION

The building blocks of digital equipment are its individual circuits. Hundreds, often thousands of them are interconnected to accomplish the operations of transferring and processing data. Actually, there are only a few different types of basic circuits, and they are used again and again in different combinations. This has the advantages of simplifying the design, increasing reliability by using only a few well-tested circuits, and making maintenance simpler and faster.

The circuits in digital equipment are simple in principle and less complicated than many circuits in radar and television sets. The types of circuits used are: logic circuits which perform logical operations with input signals, storage elements which store bits of information, and accessory circuits such as line drivers, neon indicator circuits, and others. Since it would be impractical to describe every circuit configuration now in use, only representative circuits of each type are explained here.

a. Information signals. Information in digital equipment is handled in the form of electrical signals. The transfer and processing of information is done by switching and storing information signals. The binary system is used because we have bistable (2-state, on or off) devices. Some common electronic devices (relays, vacuum tubes, crystal diodes, and transistors) perform well in bistable (2-state, or on-off) operations. Using the binary system, information signals represent the binary digits 1 and 0.

There are several ways of representing the binary 1's and 0's electrically. Some possible combinations are:

0	1
Zero Voltage	Negative Voltage
No Current	Current
Negative Pulse	Positive Pulse
Low Voltage	High Voltage
Zero Voltage	Positive Voltage
No Pulse	Pulse

Almost any circuit that has two stable states can be used as a logical element. The extreme values representing 1 and 0 are known as logic levels.

b. Switching logic. The operations carried out by a digital computer are operations of logic. Arithmetic and in fact all mathematics are rigidly based on logic. In other words, arithmetic is a systematic process of manipulating numbers involving simple operations carried out according to precise rules. If numbers are to be represented by voltage levels and pulses, some system of manipulating these voltages according to the logic rules of arithmetic must be used. Circuits which perform this function are called logic circuits.

How does switching enter into operations of logic? Do you recall the types of logic operations that can easily be performed by a switching circuit? -- To answer these and similar questions, let us briefly review the OR function and the AND function:

(1) The OR function is performed whenever any one of two or more alternate possibilities can bring about a specified result.

(2) The AND function requires that all of two or more possible conditions be present at the same time to bring about a specified result.

In chapter 2, you studied basic logic functions in terms of information only. Here we examine how physical circuits operate according to the rules of these functions. The inputs to these circuits are now going to be electrical signals representing the facts that must be logically processed. The logic blocks previously used to diagram logic functions actually represented physical circuits. Each output is an electrical signal representing the result of applying the rules of a particular logic function to a set of inputs. In other words, each output is a logical conclusion.

The switching devices commonly used in logic circuits are determined by the state of the art and the job to be done. Relays, semiconductor diodes, vacuum tubes, transistors, and magnetic cores are prevalent today. Tomorrow's devices may be different, for research is constantly seeking smaller, faster, more efficient, and more reliable switching devices.

This chapter covers the operation of logic switching circuits called gates. A gating circuit (as its name implies) acts as a swinging door that will determine whether a pulse is to pass or be stopped. For example, gates can perform AND, OR, NOT, and EXCLUSIVE OR functions.

3-2. DIODE LOGIC CIRCUITS

Some equipment uses what is called diode logic; that is, it performs most logic operations in circuits made of semiconductor diodes. Vacuum tube or transistor circuits are used primarily for building up weak or attenuated pulses.

The solid state diode, like the vacuum tube diode, has an anode and a cathode (fig 3-1). It offers very little forward resistance to the flow of electrons from the cathode to the anode; in other words, it conducts easily when the anode is made more positive than the cathode. However, when the cathode is more positive than the anode, the diode offers a very high back resistance, and practically no current can flow.

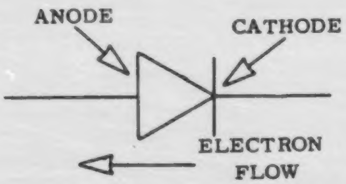


Fig 3-1. Solid state diode symbol.

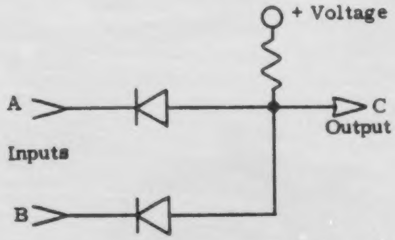


Fig. 3-2. Diode positive AND or negative OR gate.

a. Positive AND or negative OR gate. Figure 3-2 shows a diode logic circuit that can perform either the positive AND or the negative OR function. The inputs are connected in parallel, each through a separate diode to the output. The operation of the circuit depends on the voltage drop across the load resistor which, in this case, is connected to a positive voltage source. More inputs can be added, although only two are shown in the figure.

For explanation of this circuit, we assume that the logic levels are 0 volts and -10 volts. (You should remember that different equipment uses different logic level voltages to represent information.)

As the circuit in figure 3-3A shows, -10 volts are being applied to both inputs. In this circuit, both diodes are conducting; thus, both act as a short circuit for current in this direction. The output is therefore -10 volts with respect to ground for this condition. Figure 3-3B shows the equivalent circuit with both diodes acting as shorts.

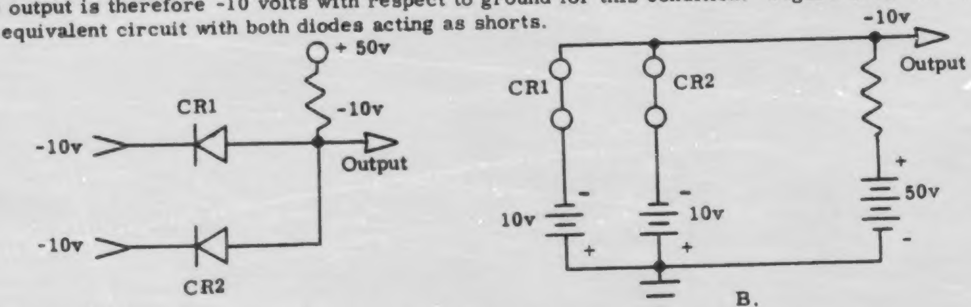


Fig 3-3. Diode circuit with both inputs -10 volts.

Figure 3-4A shows the same circuit with one input at 0 volts and the other at -10 volts. CR2 initially has a 60-volt difference in potential across it, since the +50 volts and -10 volts are connected in series-aiding. CR2 conducts and puts the anode of CR1 at -10 volts with respect to ground. This causes CR1 to act as an open, and the output is -10 volts for this condition. Figure 3-4B shows the equivalent circuit. If the -10-volt input is applied to CR1 and the 0-volt input is applied to CR2, the conditions are reversed. That is, CR1 conducts and puts the anode of CR2 at -10 volts. This causes CR2 to act as an open. The output is -10 volts for this condition also.

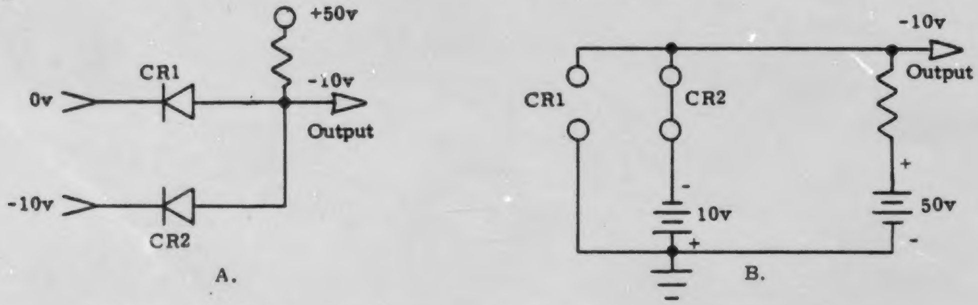


Fig 3-4. Diode circuit with one input -10 volts and one input 0 volts.

You can see that when -10 volts are applied to one input and 0 volts are applied to the other, the conducting diode shorts out the open circuit. As a result, the output is -10 volts in either case.

Figure 3-5 shows the same circuit as in figure 3-4, but with both inputs at 0 volts. Both diodes are conducting, thus acting as short circuits. For this condition, the output is 0 volts.

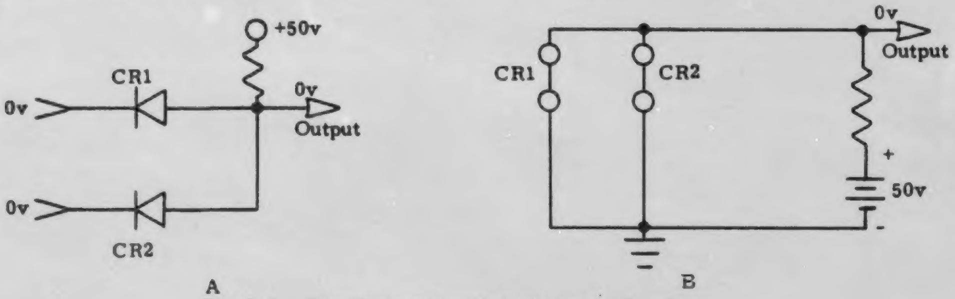


Fig 3-5. Diode circuit with both inputs 0 volts.

From the preceding discussion, it is possible to set up the device activity states or electrical truth table for the circuit in figure 3-3A. This is shown in table 3-1.

In digital-logic terminology, a high (H) is the less negative, or more positive, logic level. A low (L) is the more negative, or less positive, logic level. For example, in the preceding discussion of the diode logic gate, we noted 0 volts as the high (H) and -10 volts as the low (L). In table 3-1, substitute H for the high (0 volts) and L for the low (-10 volts); then the activity combinations table for the circuit will be as shown in table 3-2.

INPUTS		OUTPUT
A	B	C
-10v	-10v	-10v
-10v	0v	-10v
0v	-10v	-10v
0v	0v	0v

Table 3-1. Electrical states.

INPUTS		OUTPUT
A	B	C
L	L	L
L	H	L
H	L	L
H	H	H

Table 3-2. Activity combinations.

From our discussion of information signals, you will recall that a computer may use either extreme of the logic levels to represent a binary 1 or a binary 0. The voltage level which represents one of the digits may become reversed in some of the circuits during the handling operation. This is not objectionable as long as the operation remains logical and consistent, and the desired end result is obtained. If a relatively high voltage level represents a binary 1, the logic is referred to as positive logic. If a relatively low voltage level represents a binary 1, the logic is referred to as negative logic.

For the diode logic circuit in figure 3-3, we assume that the 0-volt (H) level is assigned the binary value 1; and the -10-volt (L) level is assigned to the binary value 0. As the circuit will be using positive logic, it is now possible to write a truth table for the circuit by substituting 1 for 0 volts (H) and 0 for -10 volts (L). Table 3-3 shows such a truth table.

From table 3-3, you can see that the circuit discussed performs the AND function. That is, all of the inputs must be 1 to obtain an output of 1. Since the high voltage level represents a binary 1, the function performed is called the positive AND function; and the circuit is a positive AND gate. The circuit in figure 3-3 is symbolized by the standard logic symbol for the positive AND function, as shown in figure 3-6. The Boolean equation for this circuit is AB=C.

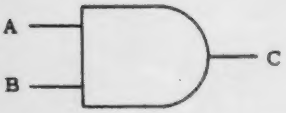


Fig 3-6. Symbol for positive AND gate.

INPUTS		OUTPUT
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Table 3-3. Truth table using positive logic.

Consider the same circuit when the -10-volt (L) level is assigned the binary value 1, and the 0-volt (H) level is assigned the binary value 0. The truth table for this condition is shown in table 3-4.

From table 3-4, you can see that the circuit now performs the OR function. That is, the output is 1 if any or all inputs are 1. Since the low voltage level represents binary 1, the function performed is called the negative OR function, and the circuit is a negative OR gate. The circuit is symbolized by the standard logic symbol shown in figure 3-7. The Boolean equation for the circuit is A + B = C.

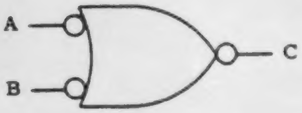


Fig 3-7. Symbol for negative OR gate.

INPUTS		OUTPUT
A	B	C
1	1	1
1	0	1
0	1	1
0	0	0

Table 3-4. Truth table using negative logic.

The small circle(s) at the input to any symbol element (logical or nonlogical) indicate(s) that the relatively low (L) input signal activates the function. Conversely, the absence of a small circle indicates that the relatively high (H) input signal activates the function.

A small circle at the symbol output side indicates that the output terminal of the activated function is relatively low (L).

From the foregoing discussion, you can see that a single circuit may perform either the AND function or the OR function, depending on the assignment of the logic levels. The circuit that you have just studied may be used as a positive AND gate or a negative OR gate.

b. Three-input positive AND or negative OR gate. Figure 3-8 shows the circuit and waveforms for three inputs to a positive AND or a negative OR gate. Just as with the 2-input gate, the 3-input gate is in parallel and connected through diodes to the output. The load resistor is connected to a positive voltage source.

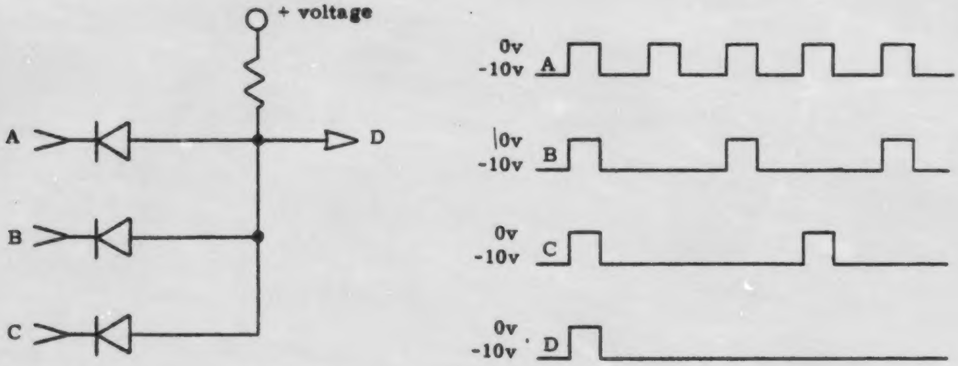


Fig 3-8. Diode circuit for a 3-input positive AND or negative OR gate.

If we assign 0 volts and -10 volts as the logic levels, the circuit acts according to table 3-5. Substitution of the term "high" (H) for the 0-volt levels and the term "low" (L) for the -10-volt levels in table 3-5 results in table 3-6.

INPUTS			OUTPUT
A	B	C	D
-10v	-10v	-10v	-10v
-10v	-10v	0v	-10v
-10v	0v	-10v	-10v
-10v	0v	0v	-10v
0v	-10v	-10v	-10v
0v	-10v	0v	-10v
0v	0v	-10v	-10v
0v	0v	0v	0v

Table 3-5. Electrical states.

INPUTS			OUTPUT
A	B	C	D
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

Table 3-6. Activity combinations.

When the 0-volt (H) level is considered the activating level and is assigned the logic value of 1, and the -10-volt (L) level is considered the inactive level and represents the logic value 0, substitution of these values for table 3-6 levels results in table 3-7.

The circuit now performs the positive AND function, and the symbol is shown in figure 3-9. The Boolean equation is ABC = D.

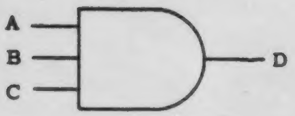


Fig 3-9. Symbol for 3-input positive AND gate.

INPUTS			OUTPUT
A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Table 3-7. Truth table using positive logic.

When the -10-volt (L) level is considered the activating level and is assigned the logic value of 1, and the 0-volt (H) level is considered the inactive level and represents the logic value 0, substitution of these values for table 3-6 levels results in table 3-8.

The circuit now performs the negative OR function, and the symbol is shown in figure 3-10. The Boolean equation is $A + B + C = D$.

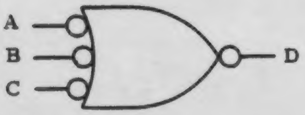


Fig 3-10. Symbol for 3-input negative OR gate.

INPUTS			OUTPUT
A	B	C	D
1	1	1	1
1	1	0	1
1	0	1	1
1	0	0	1
0	1	1	1
0	1	0	1
0	0	1	1
0	0	0	0

Table 3-8. Truth table using negative logic.

c. Positive OR or negative AND gate. We have discussed the diode logic circuit that is capable of performing either the positive AND or the negative OR function. In contrast, the circuit shown in figure 3-11 performs either the positive OR or the negative AND function.

How does the circuit in figure 3-11 differ from the circuit in figure 3-2? First, in figure 3-11 the load resistor is connected to a negative power source; second, the cathodes of the diodes are connected to the load resistor.

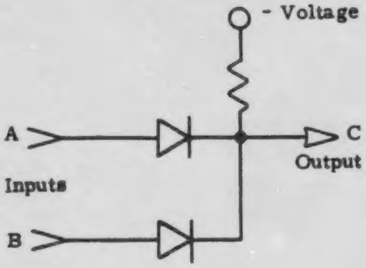


Fig 3-11. Diode positive OR or negative AND gate.

Again, for explanation of the circuit in figure 3-11, we assume that the logic levels are 0 volts and -10 volts.

Figure 3-12A shows the circuit with -10 volts applied to both inputs. Both diodes are conducting, thus acting as short circuits for current. Therefore, the output is -10 volts for this condition. Figure 3-12B shows the equivalent circuit with both diodes acting as shorts.

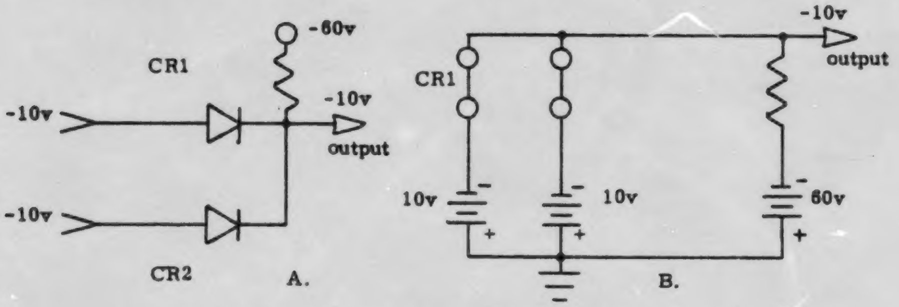


Fig 3-12. Diode circuit with both inputs -10 volts.

Figure 3-13 shows the same circuit with one input at 0 volts and the other at -10 volts. The anode of CR1 has 0 volts applied to it, and the anode of CR2 has -10 volts applied to it. This means that, initially, across CR1 there is a 60-volt difference, while across CR2 there is a 50-volt difference. CR1 conducts and shorts the output to 0 volts. This shorting action causes 0 volts to be felt on the cathode of CR2. The -10 volts in series with CR2 cause it to be biased in its high-impedance direction. Since the cathode of CR2 is positive with respect to the anode, it will not conduct but will act as an open circuit. The output of the circuit remains at 0 volts.

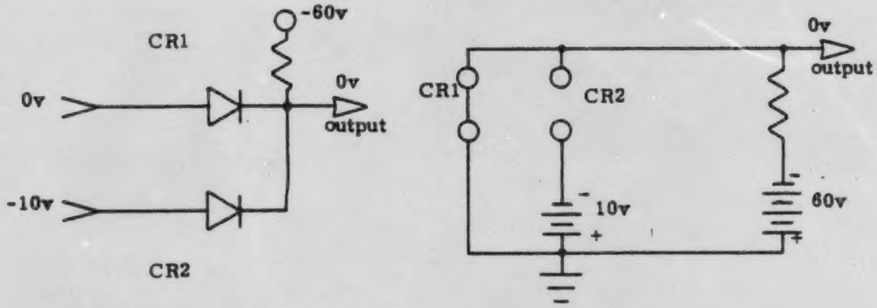


Fig 3-13. Diode circuit with one input 0 volts and one input -10 volts.

If the -10-volt input is applied to CR1, and the 0-volt input is applied to CR2, the conditions are reversed. That is, CR2 conducts and puts the cathode of CR1 at 0 volts, and again the output of the circuit is 0 volts.

Figure 3-14 shows the same circuit with both input levels at 0 volts. Both diodes conduct and short the output to 0 volts.

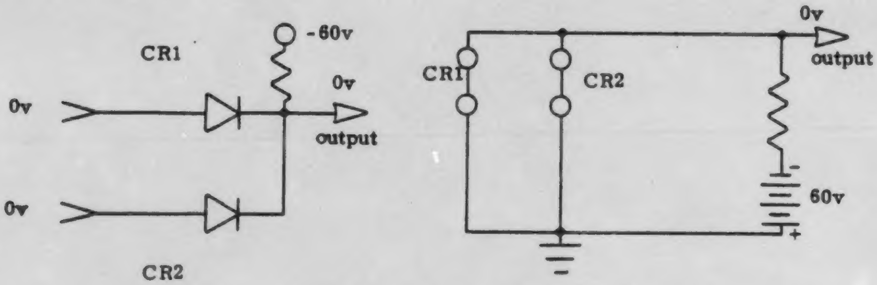


Fig 3-14. Diode circuit with both inputs 0 volts.

From the preceding discussion, it is possible to set up the device activity states or electrical truth table for the circuit in figure 3-11. This information is listed in table 3-9.

Substituting the high (H) for 0 volts and the low (L) for the -10 volts results in activity combinations for this diode logic circuit as shown in table 3-10.

INPUTS		OUTPUT
A	B	C
-10v	-10v	-10v
-10v	0v	0v
0v	-10v	0v
0v	0v	0v

Table 3-9. Electrical states.

INPUTS		OUTPUT
A	B	C
L	L	L
L	H	H
H	L	H
H	H	H

Table 3-10. Activity combinations.

Consider the diode circuit in figure 3-11 when the 0-volt (H) level is assigned the logic value 1 and activates the circuit, and the -10-volt (L) level is assigned the logic value 0 and is the inactive level. Substitution of these values in table 3-10 results in the truth table shown in table 3-11.

From table 3-11, you can see that the circuit performs the OR function. That is, the output is 1 if any or all of the inputs are 1. Since the high voltage level represents binary 1, the circuit performs the positive OR function, and is called a positive OR gate. The circuit is symbolized by the standard logic symbol for the positive OR function, as shown in figure 3-15. The Boolean equation for the circuit is A + B = C.

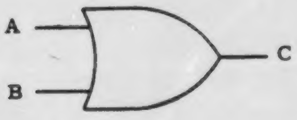


Fig 3-15. Symbol for positive OR gate.

INPUTS		OUTPUT
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

Table 3-11. Truth table using positive logic.

Consider the same circuit when the -10-volt (L) level is assigned the logic value of 1 and is the activating signal, and the 0-volt (H) level is assigned the logic value of 0 and is the inactive level. The truth table for this condition is shown in table 3-12.

From table 3-12, you can see that the circuit now performs the AND function. That is, all inputs must be 1 to obtain an output of 1. Since the low voltage level represents binary 1, the function performed is called the negative AND function, and the circuit is a negative AND gate, as represented by the standard logic symbol in figure 3-16. The Boolean equation for the circuit is AB = C.

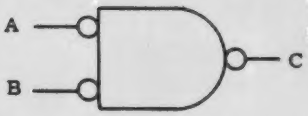


Fig 3-16. Symbol for negative AND gate.

INPUTS		OUTPUT
A	B	C
1	1	1
1	0	0
0	1	0
0	0	0

Table 3-12. Truth table using negative logic.

Again, you can see that a single circuit may perform either the OR function or the AND function, depending on the assignment of logic levels. The circuit that you have just studied may be used as a positive OR circuit or a negative AND circuit.

d. Three-input positive OR or negative AND gate. Figure 3-17 shows the circuit and waveforms for a positive OR or a negative AND gate. Just as with the 2-input gate, the three inputs are in parallel and connected through diodes to the output. The load resistor is connected to a negative voltage source.

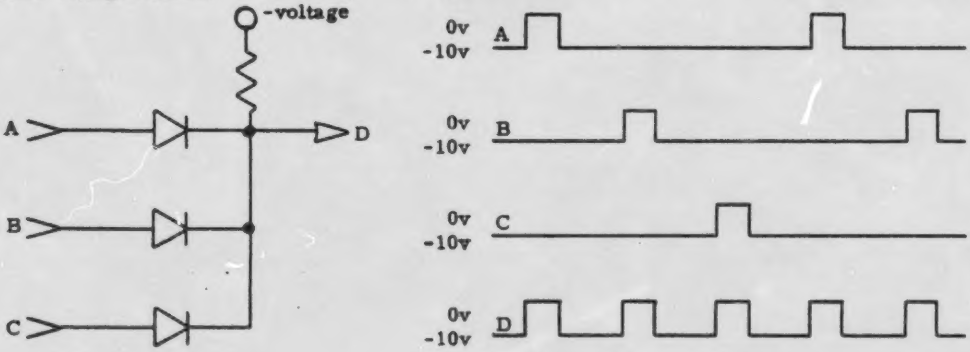


Fig 3-17. Diode circuit for a positive OR or negative AND gate.

If we assign 0 volts and -10 volts as the logic levels, the circuit acts according to the values in table 3-13.

Substitution of high (H) for the 0-volt levels and low (L) for the -10 volt levels in table 3-13 results in activity combinations shown in table 3-14.

INPUTS			OUTPUT
A	B	C	D
-10v	-10v	-10v	-10v
-10v	-10v	0v	0v
-10v	0v	-10v	0v
-10v	0v	0v	0v
0v	-10v	-10v	0v
0v	-10v	0v	0v
0v	0v	-10v	0v
0v	0v	0v	0v

Table 3-13. Electrical states.

INPUTS			OUTPUT
A	B	C	D
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	H

Table 3-14. Activity combination.

When the 0-volt (H) level is considered the activating level and is assigned the logic value of 1, and the -10-volt (L) level is considered the inactive level and is assigned the logic value of 0, substitution of these values for table 3-14 levels results in table 3-15.

With these values assigned, the circuit now performs the positive OR function, and is represented by the symbol shown in figure 3-18. The Boolean equation for the circuit is $A + B + C = D$.

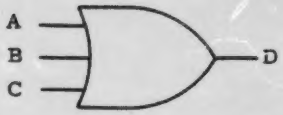


Fig 3-18. Symbol for 3-input positive OR gate.

INPUTS			OUTPUT
A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Table 3-15. Truth table using positive logic.

When the -10-volt (L) level is considered the activating level and is assigned the logic value of 1, and the 0-volt (H) level is considered the inactive level and is assigned the logic value of 0, substituting these values for table 3-14 levels results in table 3-16.

The circuit now performs the negative AND function, and is represented by the symbol in figure 3-19. The Boolean equation for the circuit is $A\ B\ C = D$.

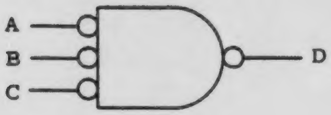


Fig 3-19. Symbol for 3-input negative AND gate.

INPUTS			OUTPUT
A	B	C	D
1	1	1	1
1	1	0	0
1	0	1	0
1	0	0	0
0	1	1	0
0	1	0	0
0	0	1	0
0	0	0	0

Table 3-16. Truth table using negative logic.

3-3. TRANSISTOR LOGIC CIRCUITS

The use of transistors in digital equipment brought about a radical change in design. In the past, vacuum tubes required large, bulky units to contain all the circuitry and power equipment; such units are no longer necessary because a transistor is much smaller than a vacuum tube. Transistors are generally housed in tiny cylinders less than 1/2 inch long. Transistors are efficient because of their small size, low power consumption, long life, and extremely flexible circuit design. As switches, they are as fast as vacuum tubes; hence, they can be used in high-speed equipment.

Modern equipment uses transistor gate circuits to perform logic functions. Transistors have the ability to amplify, and they are used to keep a signal constant through several gates. Transistors may be connected in series, parallel, or series-parallel to provide logic functions.

Several types of transistor logic circuits are used for logic gates. The type selected for a particular application will depend on power equipment, switching speed, and cost. The basic transistor logic circuits are: diode-transistor logic (DTL), resistor-transistor logic (RTL), and direct-coupled transistor logic (DCTL).

a. Diode-transistor logic (DTL). As stated earlier, the diode logic gate does not amplify the signal. To keep the amplitude constant and to prevent the diode gate from being loaded by external circuitry, a common emitter transistor circuit (gain=1) is added to the output of the diode gate. Figure 3-20 shows this type of logic network, which is a positive OR or negative AND gate. The logic symbols for this circuit are shown in figure 3-21.

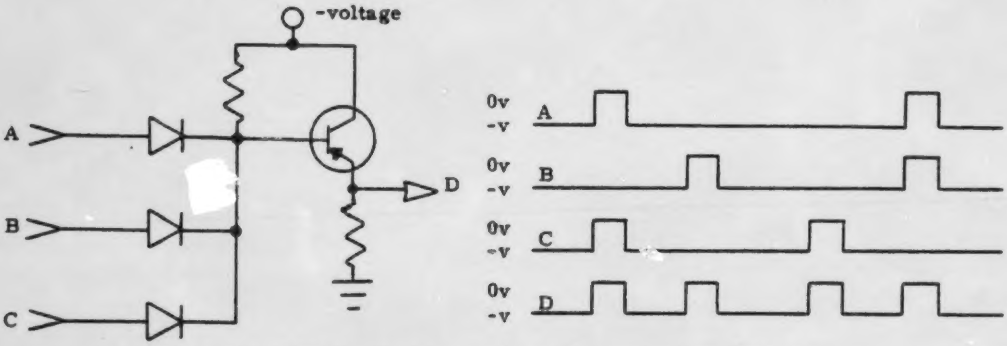


Fig 3-20. DTL circuit for a positive OR or negative AND gate.

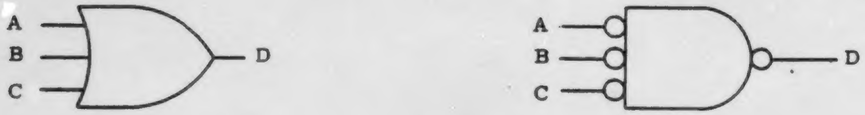


Fig 3-21. Symbols for circuit in fig 3-20.

Figure 3-22 illustrates the same type circuit used as a positive AND or negative OR gate. The logic symbols for figure 3-22 are given in figure 3-23.

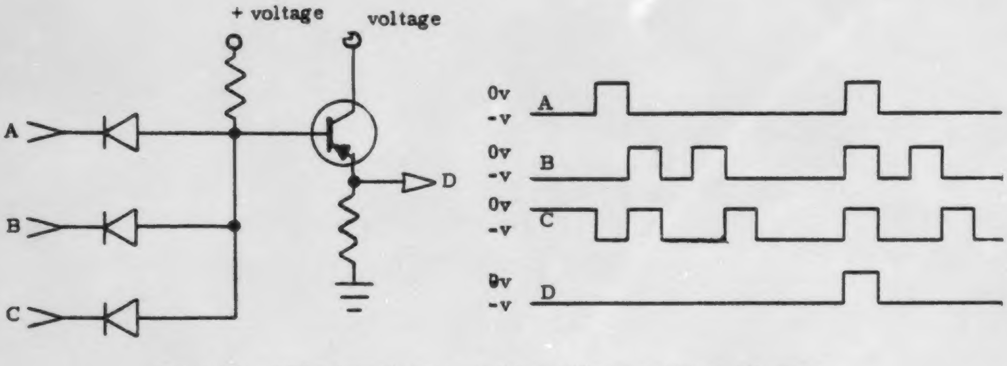


Fig 3-22. DTL circuit for a positive AND or negative OR gate.

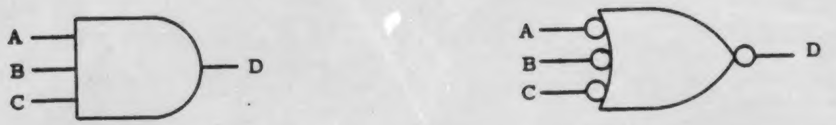


Fig 3-23. Symbols for circuit in fig 3-22.

Instead of the emitter follower as the output stage, a common-emitter or inverter circuit is generally used. This circuit (fig 3-24) is an inverted positive OR or an inverted negative AND gate. The logic symbols for the circuit in figure 3-24 are shown in figure 3-25.

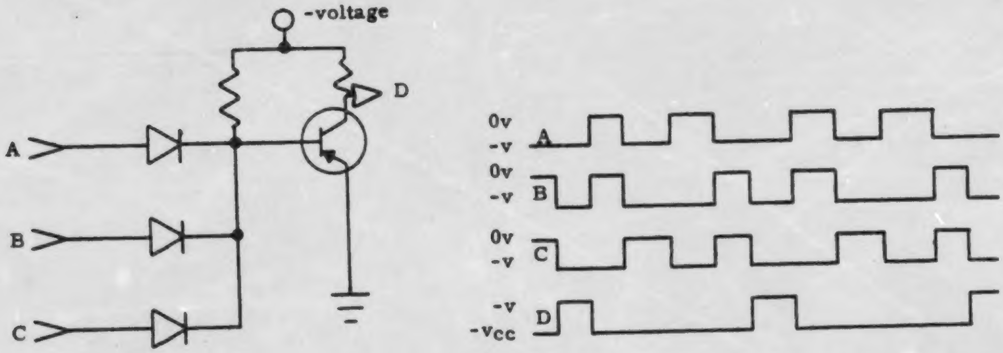

-voltage
D
A
B
C
0v
-v
A
0v
-v
B
0v
-v
C
-v
-Vcc
D

Fig 3-24. Inverted positive OR or inverted negative AND circuit.

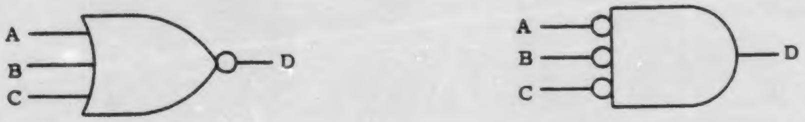


Fig 3-25. Symbols for circuit in figure 3-24.

Figure 3-26 shows the same type of circuit used as an inverted positive AND or an inverted negative OR gate. Figure 3-27 shows the logic symbols for the circuit in figure 3-26.

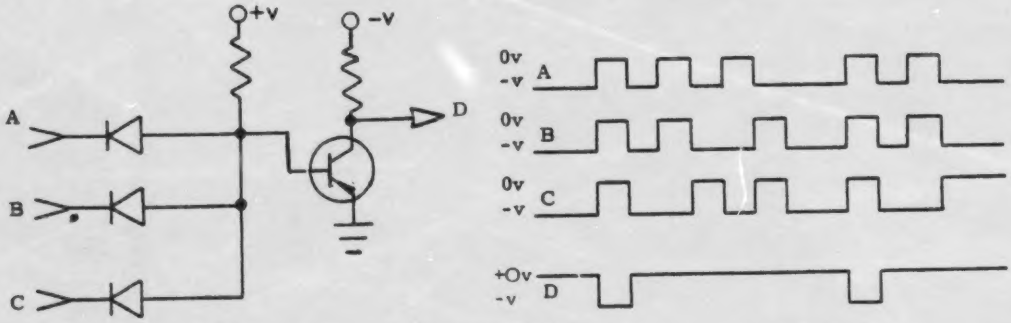

+v
-v
D
A
B
C
0v
-v
A
0v
-v
B
0v
-v
C
+0v
-v
D

Fig 3-26. Inverted positive AND or inverted negative OR circuit.

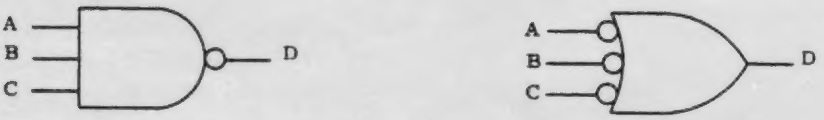


Fig 3-27. Symbols for circuit in figure 3-26.

b. Resistor-transistor logic (RTL). A resistor-transistor logic circuit is made up of a resistor gate and an inverting amplifier. Figure 3-28 shows this type of circuit with three resistors of equal value. The logic levels are assumed to be 0 volts and -2 volts. If all the inputs are at the upper level, or 0 volts, the transistor will not conduct. The resistor values are such that if one input is at the lower level of -2 volts, the transistor is driven into the saturation region. If more than one input is at the lower level, the transistor will be driven more into saturation. The output is inverted through the transistor. This circuit performs the positive AND or the negative OR function with an inverted output. The logic symbols for the circuit are shown in figure 3-29. Note that the logic symbols are the same as those in figure 3-27, but the circuit is not the same as that in figure 3-26.

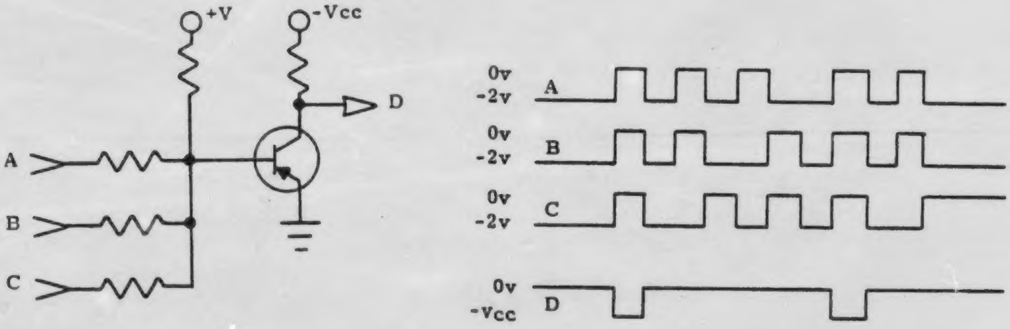


Fig 3-28. RTL circuit for a positive AND or negative OR gate with inversion.

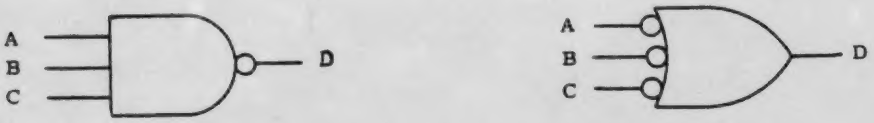


Fig 3-29. Symbols for circuit in figure 3-28.

To perform the positive OR or negative AND function with inversion, the circuit in figure 3-30 may be used. If any of the inputs is at the upper level, the transistor conducts. The resistors perform the OR function, while the transistor amplifies and inverts. The logic symbols for the circuit are shown in figure 3-31.

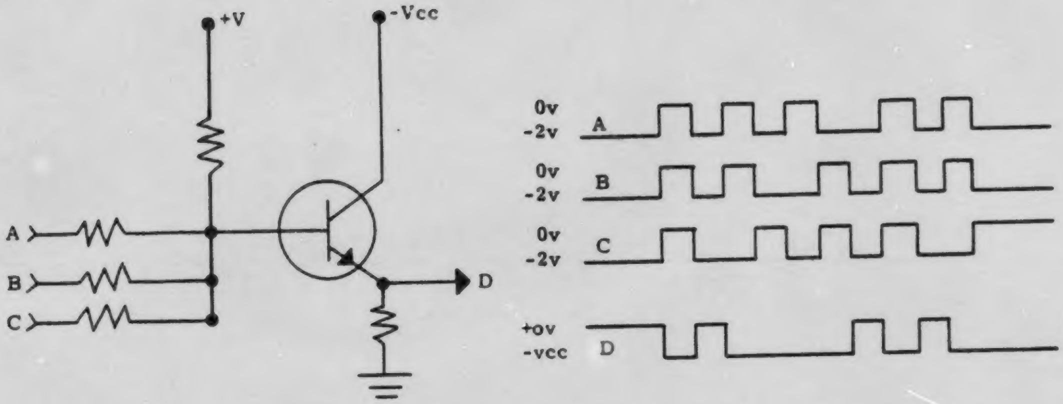


Fig 3-30. RTL circuit for a positive OR or negative AND gate with inversion.

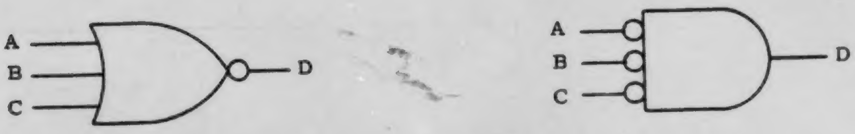


Fig 3-31. Symbols for circuit in figure 3-30.

Resistor-transistor logic circuits require the addition of RL networks, speedup capacitors, and diodes to make them work at high frequencies. Therefore, they are more complicated, less economical, and less efficient at these frequencies. However, when used with good high-frequency transistors, they are useful in high-speed computers.

c. Direct-coupled transistor logic (DCTL). Direct-coupled transistor logic, as its name implies, uses direct coupling to transfer a logic voltage level from one transistor to another. Since these circuits use only transistors and resistors, their frequency response is excellent. Logic functions can be performed with small voltage changes when DCTL circuits are used. The voltage swings may be as low as 0.2 or 0.3 volt. No level-restoring circuitry is needed since the DCTL circuit sets the upper and lower voltage levels.

Two stages of a basic transistor switch are illustrated in figure 3-32. The input signal has a 0.2-volt swing from -0.1 volt to -0.3 volt.

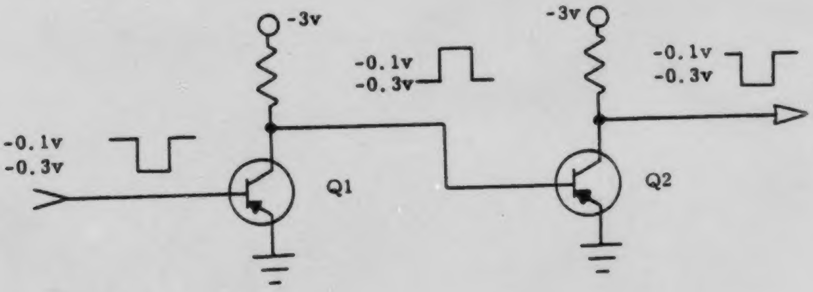


Fig 3-32. DCTL switch circuit.

A series DCTL gate consisting of two transistors in series is illustrated in figure 3-35. If the inputs, A and B, are relatively high (-0.1 volt), the output is low (-0.3 volt) -- this assumes that the gate is feeding another circuit. If either input is low (-0.3 volt), the output is still -0.3 volt. If both inputs are low (-0.3 volt), the output is high (-0.1 volt). From these facts, you can see that the series gate is either a positive input OR gate with inversion or a negative input AND gate with inversion. The logic symbols for this gate are shown in figure 3-36.

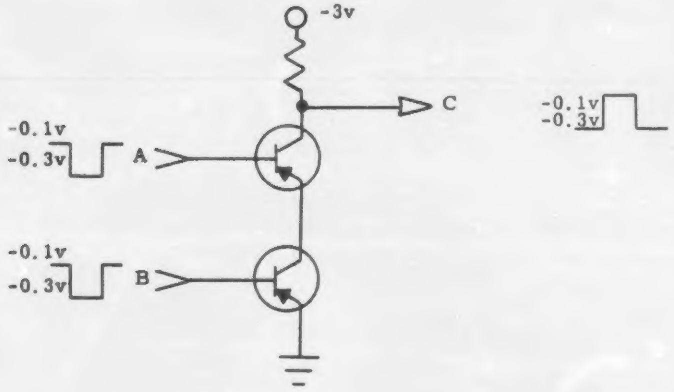


Fig 3-35. Series DCTL gate.

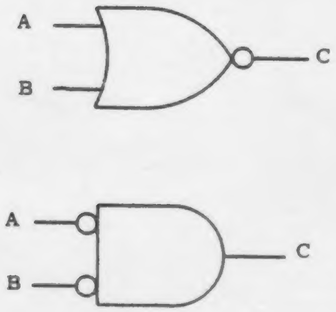


Fig 3-36. Symbols for circuit in figure 3-35.

The principles employed in the analysis of the circuit in figure 3-32 apply to all DCTL circuits.

Again, if inversion is not desired, an inverter amplifier may be added to the circuit. More transistors may be placed in series, but there is a limit to the number because the voltage drops across the transistors (small as they are) add together and reduce the voltage swing of the input.

The -0.1 volt applied to the base of Ql is insufficient to bring Ql into conduction. With Ql cut off, its collector voltage would be at V_{cc}, or -3 volts, except that the collector of Ql is directly coupled to the base of Q2 and the base-emitter junction of Q2 clamps the collector of Ql to -0.3 volt. This -0.3 volt is the voltage drop across the base-emitter junction. It is the result of I_b of Q2 flowing through the collector-load resistor of Ql (dropping -2.7 volts), and through the base-emitter resistance of Q2 (dropping -0.3 volt). Thus, the base-emitter junction of Q2 maintains the low logic level.

When the input signal goes to -0.3 volt, Ql saturates and the collector of Ql rises to -0.1 volt. This -0.1 volt is the voltage drop from collector to emitter, and is used to cut off Q2. Thus, the voltage drop across the saturated transistor (Q1) maintains the high logic level. The output voltage of Q2 will vary between -0.1 and -0.3 volt only if the output is directly coupled to an identical stage or to one which provides sufficient current through the collector resistor to maintain the -0.3 volt and when Q2 is cut off. In most other logic circuits, diodes are used to establish the logic levels. Direct-coupled methods of obtaining logic levels simplify the circuitry by eliminating the need for logic level establishing components.

A parallel DCTL gate is illustrated in figure 3-33. It has three transistors connected in parallel in a common-emitter configuration. If all three inputs, A, B, and C, are high, or -0.1 volt, the output at D will be -0.3 volt (assuming the gate is feeding another ciruit). However, if any of the three inputs is low, or -0.3 volt, the output becomes -0.1 volt. From these facts, you can see that the gate is either a positive input AND gate with inversion or a negative input OR gate with inversion. The logic symbols for this gate are shown in figure 3-34.

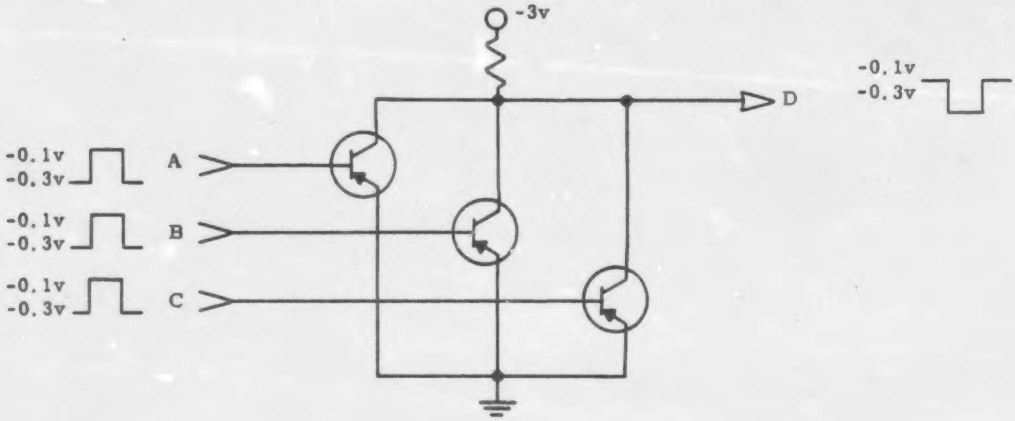


Fig 3-33. Parallel DCTL gate.

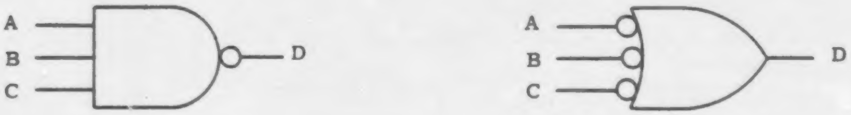


Fig 3-34. Symbols for circuit in figure 3-33.

If inversion is not desired, an inverter amplifier may be added to the circuit. More transistors can be placed in parallel to provide more inputs, but there is a limit to the number because the sum of the leakage current, I_{co}, will increase to a point where the output voltage remains too close to -0.1 volt.

The direct-coupled transistor logic circuit is simple and has low power consumption. It also has some disadvantages. The transistors and resistors must be kept within close tolerances. If many transistors are used, noise voltages are a problem. Since the voltage swings are small and the switching speed is limited, the transistors are operated at saturation.

3-4. NOT CIRCUITS

A circuit that inverts the logic of a pulse or group of pulses is called a NOT circuit, and is usually a simple inverter. A common-cathode triode or a grounded-emitter transistor amplifier constitutes a NOT circuit. This circuit is frequently used to advantage in conjunction with other switching gates to change the polarity of the signal.

An AND circuit whose output signal is inverted with respect to the input signal is called a NOT-AND, or NAND, circuit. The circuits shown in figure 3-24, 3-26, 3-28, 3-30, and 3-32 are examples of NAND circuits. Logic symbols for the NAND circuit are shown in figure 3-37.

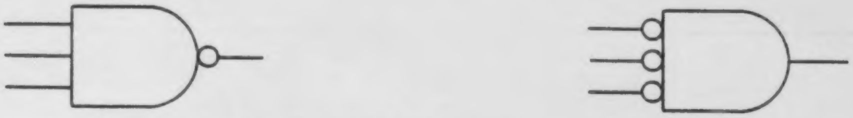


Fig 3-37. Symbols for NAND circuits.

An OR circuit whose output signal is inverted with respect to the input signal is called a NOT-OR, or NOR, circuit. The circuits shown in figures 3-24, 3-26, 3-28, 3-30, and 3-32 are examples of NOR circuits. Notice that these are the same as the NAND circuits. The function that the circuit performs depends on the logic level used to represent 1. Logic symbols for the NOR circuit are shown in figure 3-38.

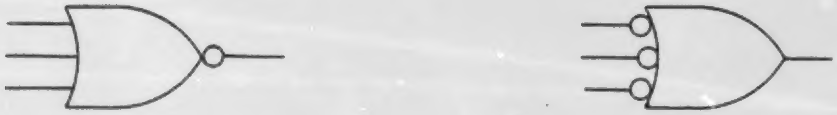


Fig 3-38. Symbols for NOR circuits.

3-5. EXCLUSIVE OR CIRCUIT

The OR function produces a specified result when any one or all of the input conditions are satisfied. Since the OR includes all combinations as well as one-at-a-time inputs, it is called INCLUSIVE OR. All the circuits discussed so far and which perform the OR function have been INCLUSIVE OR circuits. In digital logic circuits, the OR function is always "inclusive" unless otherwise specified.

A logic operation that will produce an output when either input is present, but not when both inputs are present, is called an EXCLUSIVE OR. A combination of AND and OR circuitry may be arranged to perform this logic function. Such an arrangement is shown in figure 3-39.

The Boolean equation for an EXCLUSIVE OR circuit is $A\overline{B} + \overline{A}B = C$. This says that C will be present when A or B is present, but not when both are present. A truth table for the circuit is shown in table 3-17.

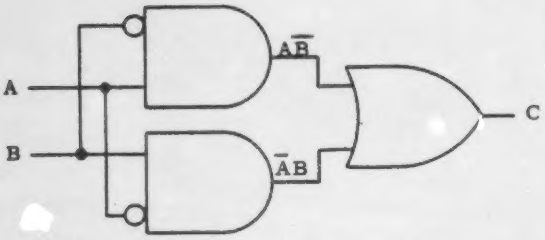


Fig 3-39. EXCLUSIVE OR logic circuit.

INPUTS		OUTPUT
A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

Table 3-17. EXCLUSIVE OR truth table.

3-6. ANALYSES

An example of an EXCLUSIVE OR circuit using DCTL is illustrated in figure 3-40.

a. Operational analysis of the circuit prior to the existence of an input signal is as follows:

(1) Transistor Q1 has approximately 0 volts applied to its base. It is grounded on its emitter and has -3 volts applied to its collector through R3. This causes transistor Q1 to be cut off.

(2) Transistor Q2 has approximately 0 volts applied to its base. It is grounded on its emitter and has -3 volts applied to its collector through R2. This causes Q2 to be cut off.

(3) Transistor Q3 has -3 volts applied to its base from R3; the emitter has -3 volts applied to it from R2; and the collector has -3 volts applied to it from R1. With the base, emitter, and collector at -3 volts, Q3 is cut off.

(4) Transistor Q4 has -3 volts applied to its base from R2; the emitter has -3 volts applied to it from R3; and the collector has -3 volts applied to it from R1. With the base, emitter, and collector at -3 volts, Q4 is cut off.

(5) The output with Q1, Q2, Q3, and Q4 cut off is the collector potential of Q3 and Q4, which is -3 volts.

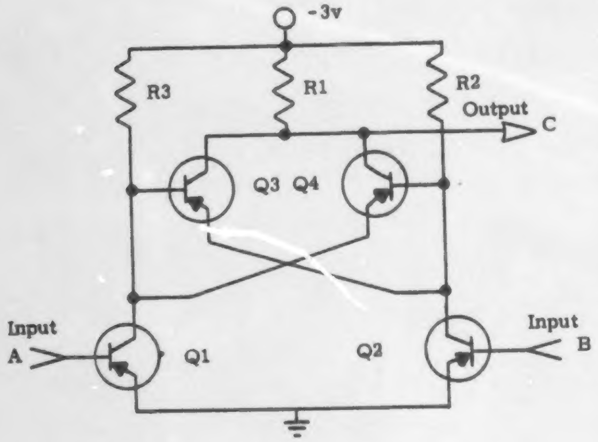


Fig 3-40. EXCLUSIVE OR circuit.

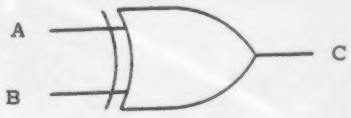


Fig 3-41. Symbol for EXCLUSIVE OR circuit.

b. Operational analysis with the injection of an input signal on the base of Q1 and no input on the base of Q2 is as follows:

(1) With a negative input pulse applied to the base of Q1, the transistor goes to saturation and acts as a short. This causes the ground potential of the emitter of Q1 to be felt at the collector of Q1.

(2) The ground potential felt at the collector of Q1 is coupled to the emitter of Q4. This now causes Q4 to have the following voltages: -3 volts on the base from R2, -3 volts applied to the collector from R1, and ground on the emitter. These voltages cause Q4 to saturate and to act as a short so that Q4's emitter potential, approximately 0 volts, will be felt at the collector of Q4. The output which is taken from the collector of Q4 will be approximately 0 volts.

(3) Transistor Q3 will remain cut off due to approximately 0 volts on the collector; —3 volts will be on the emitter, and approximately 0 volts on the base.

Note: With an input to Q2, the same operation takes place, but it will involve Q2 and Q3 instead of Q1 and Q4.

c. Operational analysis with both input signals present at the same time is as follows:

Both Q1 and Q2 go to saturation, applying 0 volts, or ground potential, to the bases and emitters of Q3 and Q4. Q3 and Q4 remain cut off, and their collector potential or output remains unchanged at -3 volts.

(The logic symbol for the EXCLUSIVE OR circuit is shown in figure 3-41.)

3-7. SUMMARY

a. A logic gate is a circuit capable of producing an output that depends on a specified type of input signal or on the coincidence of input signals. An AND gate has an output pulse when there is time coincidence of all inputs. An OR gate has an output when any one or any combination of input pulses occurs in time coincidence.

b. Semiconductor diodes and a load resistor are used to form AND and OR gating circuits. The diodes in a positive AND circuit are connected opposite in direction to those in the positive OR circuit. The supply voltage for the positive AND circuit is opposite in polarity to that in the positive OR circuit.

c. If the relatively high voltage of the logic levels represents a binary 1, the logic is called positive. If the relatively low voltage of the logic level represents a binary 1, the logic is called negative.

d. The function that a circuit performs depends on which type of logic is being used. Thus, a circuit may perform as a positive AND gate or as a negative OR gate. Likewise, another circuit may perform as a negative AND gate or as a positive OR gate.

e. A transistor may be added to a diode gate to amplify the signal. This type of logic is called diode-and-transistor logic, or DTL. A resistor-transistor logic (RTL) circuit consists of a resistor gate and an amplifier. Direct-coupled transistor logic (DCTL) circuits use direct coupling to transfer logic voltage levels. The transistors may be connected in parallel to form a positive input AND gate or a negative input OR gate. Transistors connected in series would form a negative input AND gate or a positive input OR gate.

f. A NOT circuit inverts the logic of a pulse or group of pulses. The circuit is usually a simple inverter. An AND circuit whose output signal is inverted with respect to the input signal is called a NOT-AND, or NAND, circuit. An OR circuit whose output signal is inverted with respect to the input signal is called a NOT-OR, or NOR, circuit.

g. An EXCLUSIVE OR circuit is one that will produce an output when either input is present, but not when both inputs are present.

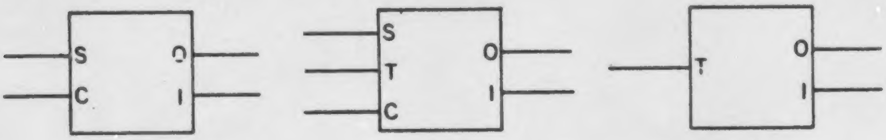
Chapter 4

LOGIC FLIP-FLOPS

4-1. INTRODUCTION

a. In our previous discussion of logic circuits, an output was present only when the required input was present. Digital equipment also requires circuits which will retain or store information supplied to it. Since the flip-flop has two stable states, it can be used to store the digits--the 0 and the 1--used in the binary number system. When the flip-flop is used to perform logic operations such as addition, subtraction, multiplication, division, and comparison, it is called a logic flip-flop.

The logic symbols for flip-flops are shown in figure 4-1. Figure 4-1A shows two inputs, set (S) and clear (C), and two outputs, one (1) and zero (0). A pulse applied to the S input will cause the outputs to be as indicated on the symbol. Conversely, a pulse applied to the C input will cause the outputs to be the NOT function of those indicated on the symbol. In figure 4-1B, a trigger (T) input has been added. A pulse applied to the T input will cause the flip-flop to change its state, so that whichever logical output was present previously will be reversed. Figure 4-1C shows a flip-flop with a single input (T). The action of the input pulse is the same as described above.



A. B. C.

Fig 4-1. Logic sybmols.

b. Many current references will label the S and C inputs as S and R inputs, with R meaning reset and S again meaning set. With this terminology, the R input acts the same way as the C input. The functioning of the flip-flop is identical.

Whether labeled S and C or S and R, an input made simultaneously on both sides of the flip-flop (S and C or S and R) will have an undetermined result. The output of the circuit will depend upon which input registered last and can only be determined by testing.

c. Another designation for S and C as inputs is J and K. Again the functioning of the flip-flop is identical, but with one significant difference. Should inputs be made on both the J and K inputs, the result will be to complement the flip-flop. The two inputs will cause this flip-flop to perform in the same way as an S and C flip-flop with an additional T input. Consequently, two simultaneous inputs in a J-K flip-flop will cause a triggering action and complement the flip-flop.

4-2. BISTABLE MULTIVIBRATOR

a. A basic bistable multivibrator is shown in figure 4-2. The switch located in the emitter circuit has been added for explanation.

Assume that the switch is open and -VCC is applied. Resistor voltage dividers R1, R3, R6 and R2, R4, R5 apply equal forward bias to Q_1 and Q_2. The voltages at the collectors are also equal. Neither transistor conducts because of the open emitter circuit.

(1) When the switch is closed, completing the emitter circuit and applying a small amount of reverse bias from the battery, both transistors start to conduct. Because of slight differences in their construction, one will conduct more than the other. (Here we assume that Q_2 conducts more than Q_1.) Thus the following actions are taking place simultaneously:

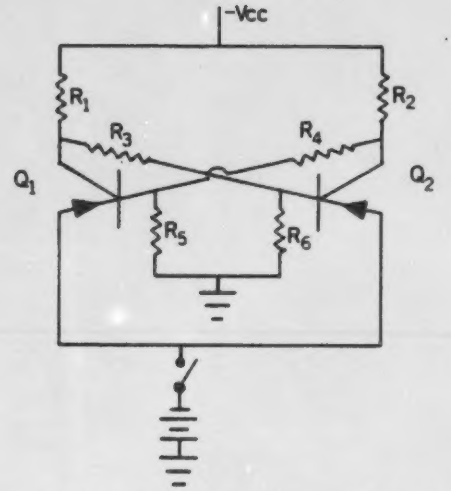


Fig 4-2. Basic bistable multivibrator.

(a) The current through Q_1 and Q_2 is increasing.

(b) The increased current through the collector resistors develops positive-going (less negative) signal voltages at the collectors. Since Q_2 is conducting more than Q_1, its signal will be larger.

(c) The signals are coupled through the divider networks to the bases of the respective transistors and act as reverse bias to oppose the increase in collector current flow. The signal at the base of Q_1 will be larger than the signal at the base of Q_2.

(2) The above action continues until the signal at the base of Q_1 is sufficient to cause its collector current to stop increasing. At this point the following conditions exist:

(a) Q_2's collector current is still increasing because the signal at its base did not reach a large enough value, but it did level off at some dc value, because Q_1's collector current is no longer changing.

(b) The signal at the base of Q_1 is still changing and therefore is continuing to reduce its collector current.

(3) As the collector current of Q_1 must now start to decrease, the following conditions will exist:

(a) The current through Q_1's collector resistor is decreasing and developing a negative-going signal at its collector.

(b) This signal is coupled through the divider network to the base of Q_2, and it acts as forward bias to increase its collector current.

(c) This increase in Q_2's collector current will continue to develop a positive-going signal voltage which is coupled to the base of Q_1 to further decrease its collector current until the reverse bias (composed of the positive-going signal and the battery) cuts off Q_1. With Q_1 cut off, its collector voltage approaches Vcc, and the divider network applies a steady forward bias to Q_2 which saturates.

(d) The flip-flop will remain in this state until a negative pulse to the base of the OFF transistor or a positive pulse to the base of the ON transistor causes the circuit to change states.

b. The circuit shown in figure 4-3 is an Eccles-Jordan multivibrator. The waveforms are included so that you will refer to them during the following explanation. Two outputs are available, each the complement of the other. One or both may be used, depending on the application.

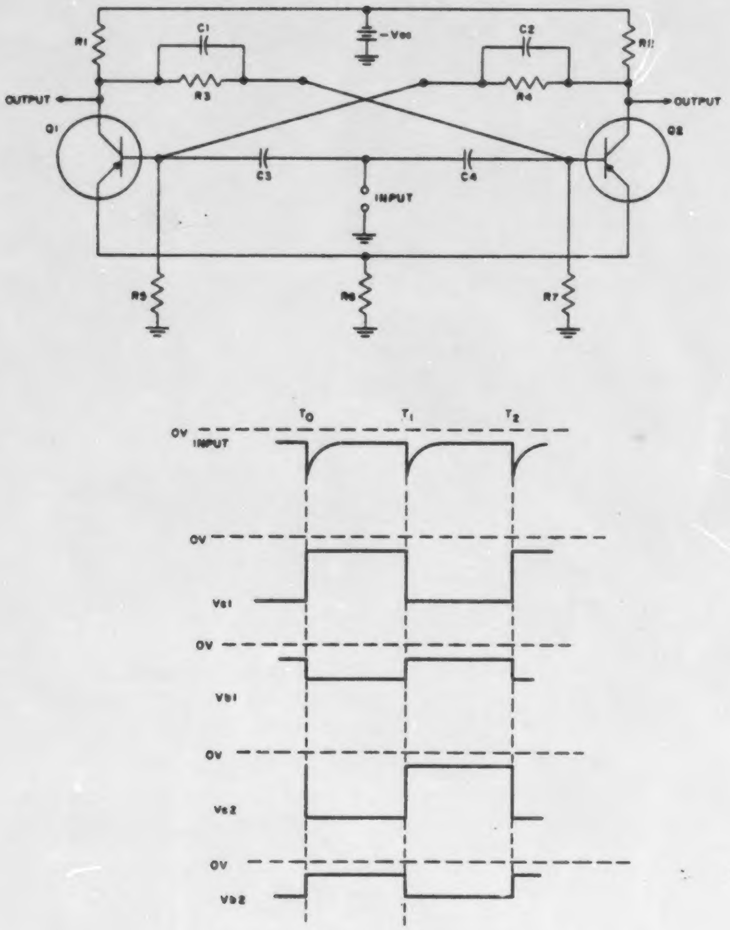


Fig 4-3. Bistable multivibrator.

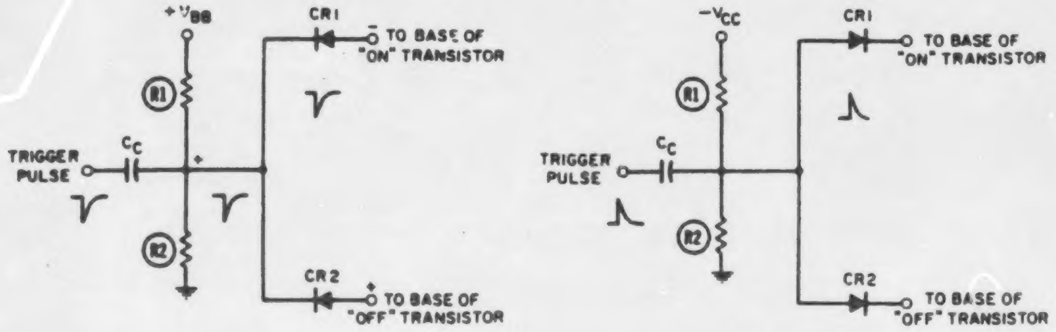
R1, R3, and R7 form the voltage divider network that develops forward bias for Q2. R2, R4, and R5 form the voltage divider network that develops forward bias for Q1. C1 and C2 are speedup capacitors used to couple fast changes in the collector circuits to the base circuits. These increase the switching speed of the circuit.

Assume that prior to time T_o Q1 is cut off, the collector voltage (V_{c1}) is near negative Vcc, and the base voltage (V_{b1}) is near zero volts. Also assume that just prior to time T_o Q2 is saturated, the collector voltage (V_{c2}) is near zero volts, and the base voltage (V_{b2}) is negative. At time T_o, a negative trigger pulse is applied to the input. This negative trigger is coupled through C3 and C4 to the bases of Q1 and Q2, and it has the effect of increasing the forward bias of both transistors. Since Q2 is already saturated, no change in its collector voltage occurs. The increased forward bias applied to Q1 causes it to start conducting and its collector voltage to change from near negative V_{cc} to slightly less negative than zero volts. This causes the base voltage of Q2 to change toward zero volts (cutoff). V_{c2} then changes toward the negative V_{cc}. This negative voltage is coupled to the base of Q1 and drives Q1 to saturation. Thus, a stable state of Q1 conducting and Q2 cutoff is reached. The flip-flop remains in this state until another negative trigger is applied at time T_1. At this time the circuit will be flipped back to its other stable state.

c. You can now see that the flip-flop has two stable states. In one state, the collector of Q1 is high and the collector of Q2 is low. The opposite is true for the other state. Thus, the output of Q1 can represent yes, true, present, etc.; and the output of Q2 can represent the opposite values--no, false, absent, etc. This 2-value system is the basis for digital logic, and for this reason the flip-flop is widely used in digital equipment.

4-3. FLIP-FLOP INPUT CIRCUITRY

The input signal applied to logic flip-flops takes on various forms, trigger pulses, pulse trains, etc. Since a flip-flop requires a sharp trigger pulse, additional circuitry is sometimes required to reshape the input signal. Also, if an input pulse is applied to the bases of both transistors from a common input source (isolated by capacitors to avoid dc interaction, as in figure 4-3), switching time will be delayed because while the OFF transistor is driven into conduction, the ON transistor is driven deeper into saturation. The turning-on action of the previously off transistor prevails, but must first overcome the effects of the ON transistor being driven deeper into saturation. Therefore increased input signal strength is required, and the rise and fall times of the output signal are increased. By adding pulse-steering diodes (fig 4-4), the input pulse is directed to the transistor that is to be affected.


+V_BB
CR1
TO BASE OF "ON" TRANSISTOR
R1
TRIGGER PULSE
Cc
R2
CR2
TO BASE OF "OFF" TRANSISTOR
−Vcc
CR1
TO BASE OF "ON" TRANSISTOR
R1
TRIGGER PULSE
Cc
R2
CR2
TO BASE OF "OFF" TRANSISTOR

(A) Negative.

(B) Positive.

Fig 4-4. Pulse-steering diode circuits.

a. Pulse-steering circuit operation. Assume the desired input pulse is negative (fig 4-4A). The pulse passes through coupling capacitor C_c, and through the voltage-divider R1-R2, which had been keeping the cathodes of the diodes at a positive potential. Diode C_{R1} has been reverse-biased, because the ON transistor has a significant negative base voltage. For comparable reasons, C_{R2} has been conducting because of its forward bias. Thus, when the negative trigger pulse comes through C_c, reverse-biased C_{R1} prevents the pulse from being applied to the base of the ON transistor. However, forward-biased diode C_{R2} permits the negative trigger pulse to pass through easily, and to be applied to the base of the OFF transistor, turning it on in the conventional fashion. After the switching action, the pulse-steering diodes change bias accordingly, so that the next trigger pulse would be blocked by C_{R2}, but would easily pass through C_{R1}. Note also that a positive trigger pulse applied to this steering circuit, regardless of the state of the flip-flop, increases the reverse bias on the diodes, and hence has no triggering effect on the circuit.

For positive-connected pulse steering (used with N-P-N transistors), the circuit would be set up as shown in fig 4-4B. Note that the voltage-divider polarity is reversed, and the steering diode directions are changed.

b. Combination pulse-steering and differentiation circuit operation. In circuits which utilize a wide pulse train (rather than a single or occasional sharp pulse), the input circuit shown in figure 4-5 is often used. An increase in switching action is made possible by the differentiating action of the steering-diode circuitry.

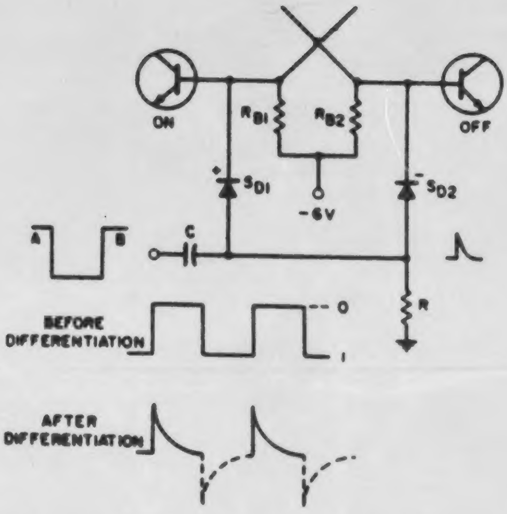


Fig 4-5. Differentiating action in steering-diode circuits.

Base resistors R_{B1} and R_{B2} are returned to -6 volts. The ON transistor has a positive base (forward bias), so that the cathode of S_{D1} is positive and therefore reverse-biased. The OFF transistor has a negative base (reverse bias), so that the cathode of S_{D2} is negative and therefore conducting. The point common to both steering diodes is at the junction of C and R. These components form a differentiating circuit for the input pulse. The RC time constant is chosen to produce a steep positive spike of short duration, which passes through the steering diode (S_{D2} in this case) to initiate switching action. The negative spike produced (dotted portion of the waveform) simply reverse-biases both steering diodes and does not affect circuit operation.

For application in circuits which use PNP transistors, the steering diode directions are changed, and the negative portion of the differentiated waveform is used to switch the flip-flop.

4-4. THREE-INPUT FLIP-FLOP

a. Figure 4-6 illustrates a flip-flop circuit with three inputs for triggering. This circuit is activated by negative trigger pulses. A negative-going input signal applied at A always causes the flip-flop to change states. A is the complementing input. A trigger pulse applied at B causes the output voltage at D to be low. A trigger pulse applied at C causes the output voltage at E to be low.

b. Refer to figure 4-6 during the following analysis of the circuit. The bistable multivibrator consists of two transistors, Q1 and Q2. Each transistor collector output of the flip-flop is fed back through a complementary emitter follower to the base of the other transistor. The circuit constants are chosen so that, in the stable state, Q1 is either cut off or saturated, and Q2 is in the complementary state.

An input trigger pulse applied to input B causes forward bias of the emitter-base junction of Q1. This causes the collector of Q1 to be at approximately zero volts, or a high voltage. This high voltage is fed through the complementary emitter follower, Q5 and Q6, to the output at E, and at the same time through C2 and R8 to reverse-bias the emitter-base junction of Q2. The collector output of Q2, because of Q2 being cut off, is -12 volts, or a low voltage. This voltage is fed through the complementary emitter follower, Q3 and Q4, to output D, and at the same time through R1 and C1 to the base of Q1. This completes the regenerative loop, and the flip-flop will remain in this state until trigger pulse is applied to input C or to input A.

The application of a trigger pulse at input C causes forward bias of the emitter-base junction of Q2. This causes the collector of Q2 to be at zero volts, or a high voltage. This high voltage is fed through the complementary emitter follower, Q3 and Q4, to output D, and through C1 and R1 to the base of Q1. This causes Q1 to cut off. The collector output of Q1, due to cutoff, is -12 volts, or a low voltage. This voltage is fed through the complementary emitter follower, Q5 and Q6, to output E, and at the same time through R8 and C2 to the base of Q2. This completes the regenerative loop, and the flip-flop will remain in this state until a trigger pulse is applied to input B or input A.

The complementing input A is used to reverse the state of the flip-flop with each application of a negative trigger pulse. Because of the diode configuration, CR3 and CR4, the negative pulse will be steered to the base of the cutoff transistor. If Q2 is conducting, the pulse is applied to the base of Q1. This changes the state of Q1 from cutoff to conduction and, through the regenerative loop previously described, changes the state of Q2 from conduction to cutoff. Each successive negative pulse at A reverses the states of Q1 and Q2 in the same manner, and therefore changes the output voltage levels at D and E.

c. Referring to the waveforms in figure 4-6, note that the pulse applied to input B at time T_1 changes the voltage levels at outputs D and E. Also, note that the pulses at T_2 and T_3 do not change these levels. This is so because the base of Q1 is already negative and Q1 is conducting. When a negative pulse is applied at time T_4 to input C, the voltage levels at D and E are reversed, but the following pulses applied at times T_5 and T_6 have no effect. In contrast, when a negative pulse is applied to input A at times T_7, T_8, T_9, and T_{10}, each consecutive pulse triggers the flip-flop and changes the voltage levels at D and E. Figure 4-7 shows the logic symbols for the 3-input flip-flop.

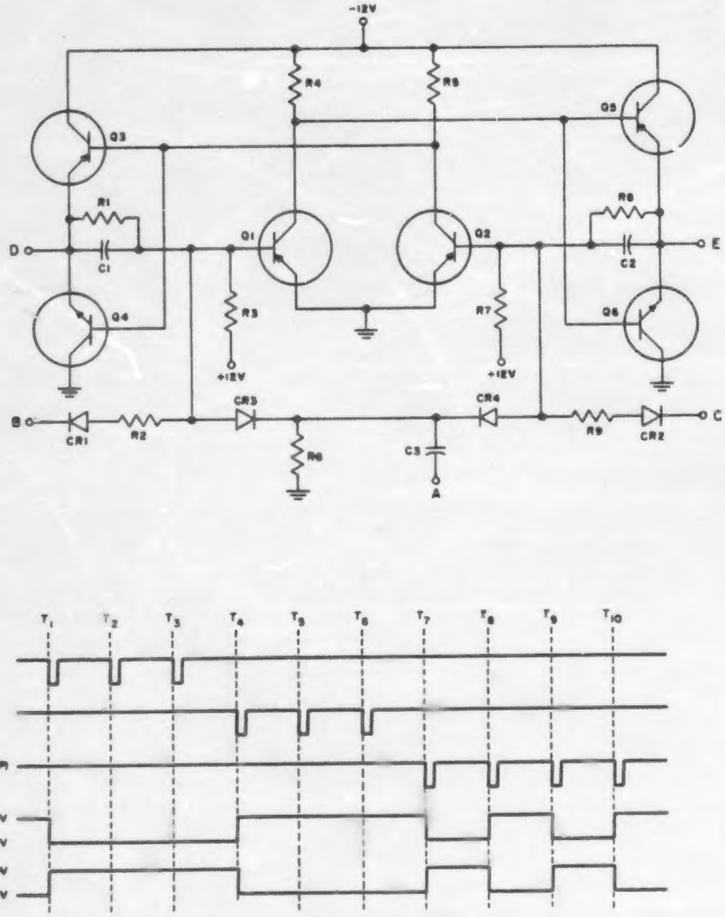


Fig 4-6. Three-input flip-flop.

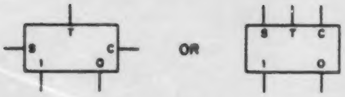


Fig 4-7. Logic symbols for 3-input flip-flop.

4-5. LOGIC FLIP-FLOP WITH LOGIC GATE INPUTS

a. How does the logic flip-flop differ from the basic Eccles-Jordan multivibrator? Figure 4-8 shows a basic flip-flop with modifications that permit it to be used in logic circuits. These modifications, which amount to addition, are:

(1) Logic circuits at the inputs to insure that the flip-flop will be triggered at the desired time.

(2) Circuits for presetting the flip-flop to a desired state.

(3) Differentiating circuits to give sharp trigger pulses.

(4) Visual indicators of the state of the flip-flop.

(5) Limiting circuits to establish the desired logic levels.

b. For the following circuit analysis, refer to figures 4-8 and 4-9. For explanation, we assume that a high voltage at the output (0 volts) will represent the designated function; and a low output (-10 volts), the NOT function.

Transistors Q3 and Q4 form the multivibrator. Q3 is the ONE side transistor and Q4 is the ZERO side transistor. R1 and R2 are collector-load resistors. R2, R6, and R9 form the voltage divider network for forward biasing Q3. R1, R5, and R10 form the voltage divider network for forward biasing Q4. The important portion of the forward bias for operation of this circuit is developed across R9 and R10. C1 and C2 will couple fast collector changes to the transistor bases in order to increase the switching speed of the flip-flop.

The inputs to the flip-flop consist of SET and CLEAR circuits and logic input circuits. The logic circuits in this case are AND gates. CR5, CR6, and R7 form the AND gate that feeds the ONE side transistor and triggers the flip-flop to the ZERO state. CR8, CR9, and R12 form the AND gate that feeds the ZERO side transistor and triggers the flip-flop to the ONE state. The CLEAR input is fed to C4 and the SET input is fed to C6. These inputs make it possible to preset the flip-flop to a desired state.

C3, R13, C5, and R14 are differentiating networks that differentiate the outputs of the AND gates. C4, R13, C6, and R14 form the differentiating networks for the CLEAR and SET inputs. R8, R13, R11, and R14 form voltage divider networks that place negative potentials on the anodes of CR7 and CR10. This negative potential allows them to conduct only on the positive spike of the differentiated wave and permits CR7 and CR10 to perform their functions as limiting diodes, clipping the negative spikes.

Transistors Q1 and Q2 are emitter followers. The outputs are taken from their emitters. CR1, CR2, CR3, and CR4 are limiting diodes that maintain the logic levels at 0 volts and 10 volts. The outputs are connected to neon indicators so that the state of the flip-flop can be determined by visual inspection. These indicators are not shown in figure 4-8.

72

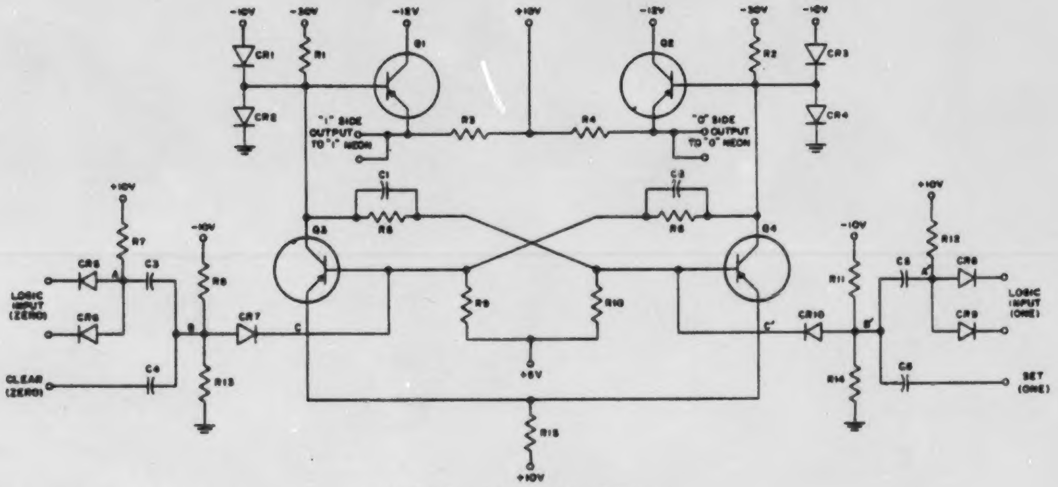

-10V
-30V
-12V
+10V
-12V
-30V
-10V
CR1
R1
Q1
Q2
R2
CR3
CR2
CR4
"1" SIDE OUTPUT TO "1" NEON
R3
R4
"0" SIDE OUTPUT TO "0" NEON
C1
R5
C2
R6
+10V
R7
-10V
Q3
Q4
-10V
+10V
R12
CR5
A
C3
R8
R11
C5
A'
CR8
LOGIC INPUT (ZERO)
CR6
R9
R10
LOGIC INPUT (ONE)
CR9
B
CR7
C
C'
CR10
B'
+6V
CLEAR (ZERO)
C4
R13
R14
C6
SET (ONE)
R15
+10V

Fig 4-8. Logic flip-flop.

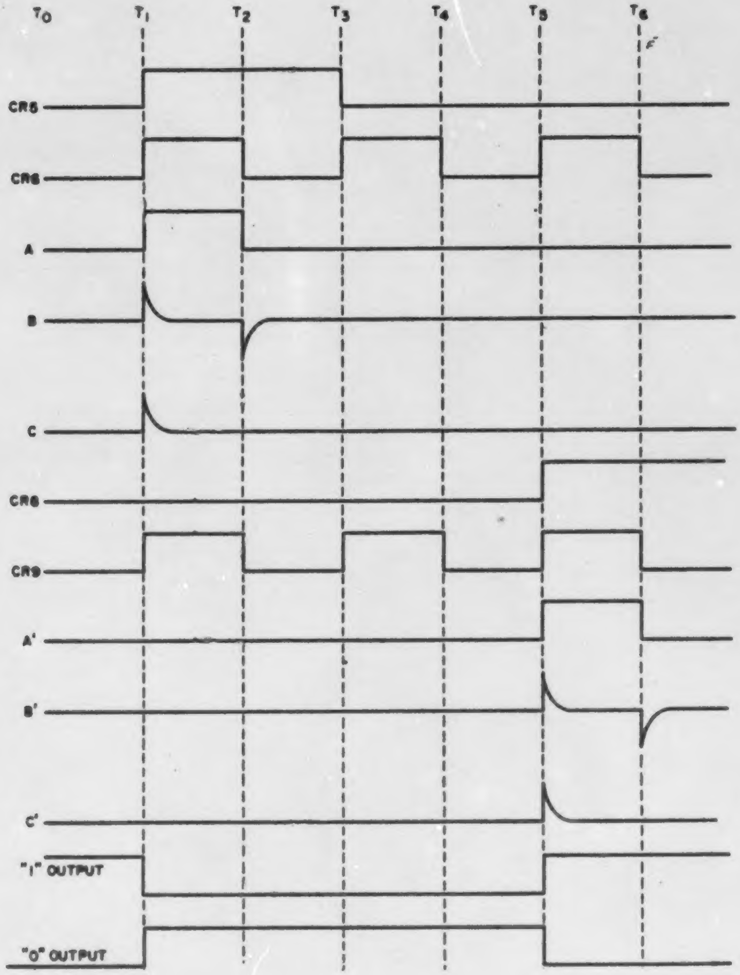


Fig 4-9. Waveshapes for logic flip-flop.

81

c. Now we analyze the function of this flip-flop during one cycle of operation. Refer to the circuit in figure 4-8 and the waveshapes in figure 4-9.

At time T_0, the flip-flop is in the ONE state. This means Q3 is conducting and Q4 is cut off. The ONE-side output is at 0 volts and the ZERO-side output is at -10 volts. At time T_1, signals are applied to CR[illegible] CR6, as shown in figure 4-9.

The signals A, B, and C in figure 4-9 are the signals at points A, B, and C in the circuit in figure 4-8. Signal A is the output of the AND gate. Signal B is the output of the differentiating network. Signal C is the output of the limiting diode. Since both the ONE-side and the ZERO-side input circuits and their waveshapes will be the same, it is sufficient to explain only one input circuit.

The input signals to the circuit are both high during the time from T_1 to T_2. (This is the only time an output from the AND gate will be present, as illustrated by signal A in figure 4-9.). Signal A is then differentiated by C3 and R13 (signal B), and the negative spike is clipped by CR7 (signal C).

The positive spike of the signal at C is applied to the base of Q3 at time T_1 and will cut off Q3. The collector voltage of Q3 goes to a negative potential. This negative change is coupled by C1 to the base of Q4, causing Q4 to conduct. The collector voltage of Q4 decreases toward zero volts. This decrease is coupled by C2 to the base of Q3 and keeps Q3 cut off.

With Q3 cut off, the collector voltage is at -10 volts because of the logic level establishing diode CR1. This voltage (a low) is applied to the base of Q1, and the output of -10 volts is taken from the emitter of Q1. This is the ONE-side output.

After time T_1, Q4 is saturated and the collector is at 0 volts because of the clamping action of CR4. This voltage (a high) is applied to the base of Q2, and the output of 0 volts is taken from the emitter of Q2. This is the ZERO-side output. The flip-flop is now in the ZERO state, and remains in this stable state--the ZERO state--until time T_5. Then the inputs to CR8 and CR9 (fig 4-9) activate the logic input (ONE) gate. Signals A', B', and C' are generated and a positive trigger (C') is applied to the base of Q4. This will cut off Q4 and trigger the flip-flop to the ONE state, with Q3 conducting and Q4 cut off. The multivibrator action is the same as was discussed in triggering the flip-flop to the ZERO state.

The logic symbols for the logic flip-flop are shown in figure 4-10.

The symbol in figure 4-10A is used when the logic gates are physically integral with flip-flop functions. The symbol in figure 4-10B is used when the logic gates are physically separated from the flip-flop functions.

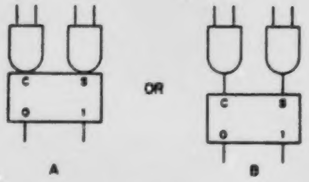


Fig 4-10. Logic symbol for flip-flop with logic gate inputs.

4-6. SUMMARY

a. The logic flip-flop has two stable states. It is used to temporarily store binary 1 or binary 0. When its output represents a binary 1, it is said to be in the ONE state. When its output represents a binary 0, it is said to be in the ZERO state.

b. A bistable multivibrator circuit with modifications is used as a logic flip-flop. The basic circuit is modified by using input logic gates, differentiating networks, logic level-setting circuits, circuits for presetting, and state indicators.

c. The complementing flip-flop uses pulse-steering circuits to enable it to be triggered by pulses from a common source.

d. The 3-input flip-flop has a complementing input plus separate inputs to each side of the flip-flop.

Chapter 5

NONLOGIC CIRCUITS

5-1. INTRODUCTION

Not all circuits in digital equipment perform logic functions. Circuits are also needed to amplify, time, reshape, delay, invert, or restore signal levels. Circuits that perform these functions are presented in this chapter. Representative circuits are used as examples, since it is impractical to discuss every circuit variation in use today.

Nonlogic circuits perform important functions. Their job is to support the logic circuits in the accomplishment of digital functions. Some of these circuits make the internal workings known to the operator through visual monitoring devices; others extract information from logic circuits and convert it into usable outputs to operate various displays or other output devices.

5-2. EMITTER FOLLOWER

a. The emitter follower is a nonlogic circuit which uses the common-collector configuration. This circuit is used mainly as an impedance-matching device and as a current source. It has no phase inversion, it has relatively low power gain, and it causes only a slight alteration of the input signal voltage level.

b. Figure 5-1 is the schematic diagram of a basic emitter-follower. Note that the collector is connected to a negative source of -6.5 volts. This will prevent the base-collector junction from becoming forward-biased as long as the input signal does not become more negative than -6.5 volts.

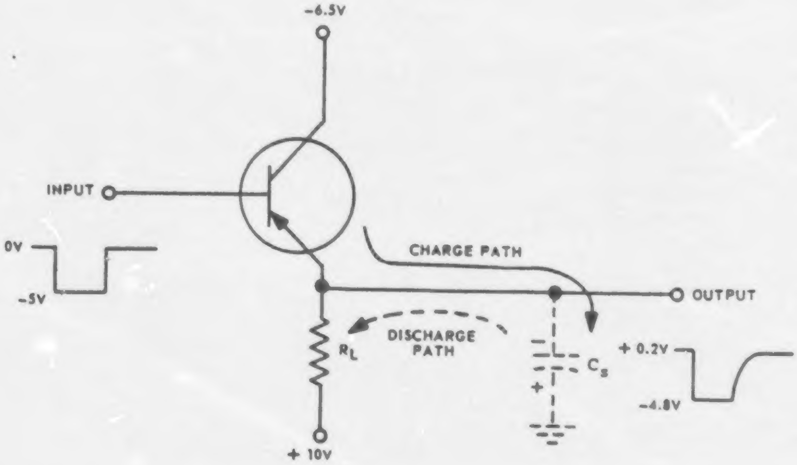


Fig 5-1. Basic emitter-follower.

c. Assuming a 0-volt input, the base-emitter junction conducts and the emitter supply voltage is divided between R_L and the forward resistance of the base-emitter junction. Under this condition, the output of the circuit is approximately +0.2 volt with respect to ground.

When the input signal goes in the negative direction, it increases the forward bias on the base-emitter junction and causes an increase in collector-emitter current. The change at the input is immediately reflected in the output due to the resulting small resistance of the base-emitter junction. The output voltage will increase to -4.8 volts. The stray capacitance (C_s) in the line is across the output and charges to -4.8 volts. The charging path is through the low impedance of the transistor; thus, the voltage will change rapidly at the leading edge of the pulse.

When the input signal changes back to 0 volts, the output voltage cannot follow the change immediately, due to the exponential discharge rate of C_s through the load resistance, as shown in figure 5-1. This is a relatively higher resistance than the charge path.

d. Notice that the voltages which represent the logic levels have been changed from 0 and -5 volts to +0.2 and -4.8 volts. When only one stage is used in an emitter-follower configuration, this change in the voltage levels can be considered negligible; but it becomes more evident when the signal is passed through several emitter-followers. To compensate for such change, a voltage divider circuit is added, as in figure 5-2. By using the proper ratio of R1 to R2, the voltage at the base connection will be approximately -0.2 volt when the input signal is at 0 volts. This added forward bias causes an increase in emitter current, resulting in an upper voltage level at the output of approximately 0 volts.

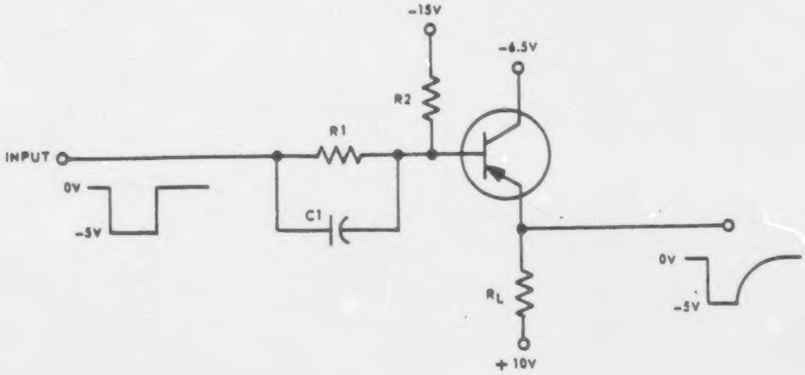


Fig 5-2. Emitter-follower with voltage divider.

The addition of a fast coupling capacitor (C1) across R1 compensates for the slower rise time caused by the transistor input capacitance. With C1, the initial input signal will be immediately felt on the base.

e. In circuits requiring fast rise and fall times, a complementary emitter-follower configuration may be used. The complementary emitter-follower circuit uses a PNP and an NPN transistor in push-pull (fig 5-3). This circuit provides a relatively short time-constant charge and discharge path for the stray capacitance. In the quiescent state, in this case 0 volts input, each transistor is biased by individual voltage dividers-consisting of R1 and R2, R3 and R4. The resistors are selected so that equal currents flow through each transistor, resulting in a 0-volt output. When the input changes to -5 volts, Q2 is reverse-biased and the forward bias on Q1 is increased. The leading edge of the input pulse is fast-coupled to the bases by C1 and C3. C_s charges rapidly through the low resistance of Q1. When the input again changes to 0 volts, the charge on C_s is felt on the emitter of Q2 as a forward bias. Therefore C_s is rapidly discharged through the low resistance of Q2. --Remember that C_s in the emitter-followers shown in figures 5-1 and 5-2 discharged through the load resistance and caused the output pulse to have a slow rise time. The complementary emitter-follower in figure 5-3 provides a low-resistance discharge path for C_s, and gives the output pulse a fast rise time.

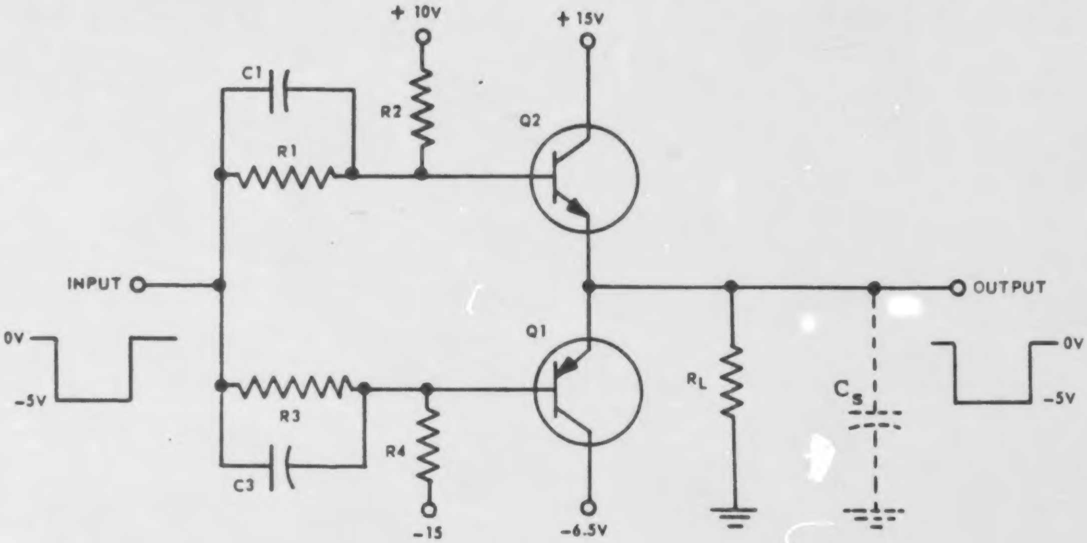

+ 10V
+ 15V
C1
R2
Q2
R1
INPUT
OUTPUT
0V
-5V
Q1
R3
R4
C3
-15
-6.5V
R_L
C_S
0V
-5V

Fig 5-3. Complementary emitter-follower.

5-3. PULSE AMPLIFIER

a. The pulse amplifier is a nonlogic circuit used to increase the driving capabilities of a pulse, to increase the amplitude of a pulse, or to narrow a pulse width that has become excessive.

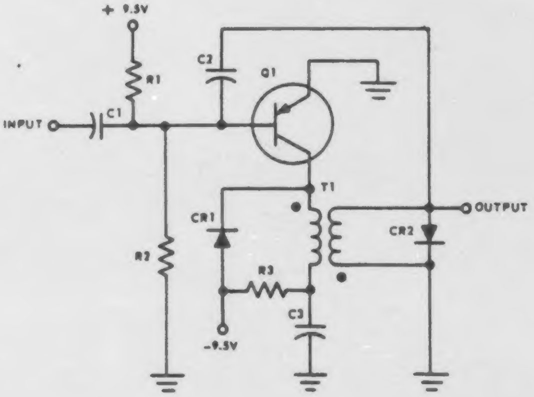

+ 9.5V
C2
Q1
R1
INPUT
C1
T1
CR1
OUTPUT
CR2
R2
R3
C3
-9.5V

Fig 5-4. Pulse amplifier.

b. Figure 5-4 shows the schematic diagram of a pulse amplifier. The circuit consists of one transistor (Q1) connected in a common-emitter configuration to amplify the signal and give the necessary power gain. The circuit also contains a pulse transformer (T1), to bring the output signal in phase with the input signal and to determine the pulse width of the output.

c. At quiescence, the input is at ground potential, Q1 is at cutoff, and the output is at ground potential. With the application of a negative pulse at the input, Q1 becomes forward-biased and turns on. Current starts to flow from the -9.5-volt supply through the transistor to the emitter. The current flow in the collector circuit (T1 and R3) causes the collector to rise from -9.5 volts toward 0 volts. The changing current in the primary transformer T1 produces an expanding magnetic field which induces a voltage across the secondary. This output will be an increasing negative potential as long as the current through the primary of the transformer is increasing. When the current flow through the primary of the transformer drives the core of T1 to saturation, the voltage induced across the secondary decreases to 0 volts. Since the induced voltage in the secondary will fall off before the end of the input pulse, the width of the output pulse is not dependent on the width of the input pulse. (For this reason, the pulse amplifier may be used to narrow a pulse whose width has been excessive.) Current will continue to flow in the transistor as long as the negative voltage is applied to the input. When the input returns to ground potential, no current flows in the circuit, the magnetic field collapses, and the circuit is once again in the steady state.

d. The current flow through the primary would not normally reach maximum immediately, because Q1 is not fully conducting at the first instant. The addition of C2 in this circuit causes the circuit to reach its maximum conduction state very rapidly. When the current in the secondary starts to change, the resultant voltage produces a feedback to the base of Q1 through C2 and puts Q1 into saturation, thus resulting in a rapid rise time.

e. As the magnetic field collapses when Q1 is cut off, a negative overshoot is induced in the primary of T1. Diode CR1 prevents the presence of this overshoot at the collector. It conducts at this time through R3 and the primary, and dampens the overshoot. The collapsing field also induces a positive pulse in the secondary, but CR2 limits it to 0 volts. C3 is a decoupling capacitor.

5-4. RELAY DRIVER

The relay driver is a nonlogic circuit used to energize a relay which, in turn, will switch high currents and voltages.

Figure 5-5 is the schematic diagram of a relay driver. The circuit consists of a grounded-emitter amplifier and associated components.

With the input to the driver at ground level (0 volts), Q1 is turned off, thereby presenting a high impedance. No current flows in the circuit, and therefore the relay is not energized. When the input is switched to the negative level, Q1 becomes saturated and presents a low-impedance path to the flow of current. As current flows through the relay coil, the relay becomes energized and the contacts are closed, thereby performing the switching function.

CR1 is used to limit the negative overshoot from the relay coil.

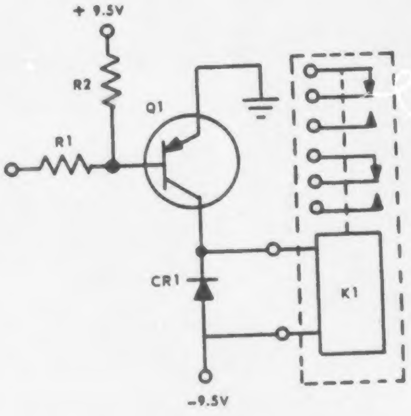


Fig 5-5. Relay driver.

5-5. LEVEL RESTORER

a. The level restorer serves to restore pulse voltages to a desired level.

b. Two cascaded common-emitter stages, as shown in figure 5-6, amplify the negative input pulse so that the output is in phase with the input. In this example, the output pulse limits are approximately ground potential and -12 volts.

c. Assume that a signal pulse which should be -12 volts has deteriorated to -6 volts. With an input signal of less than -6 volts, Q1 is at cutoff. Resistors R3 and R4 divide the source voltages of -12 volts and +12 volts so that the base of Q2 is approximately -3 volts. This forward bias is sufficient to have Q2 conducting at saturation. In this condition, the output is at approximately ground potential, or 0 volts.

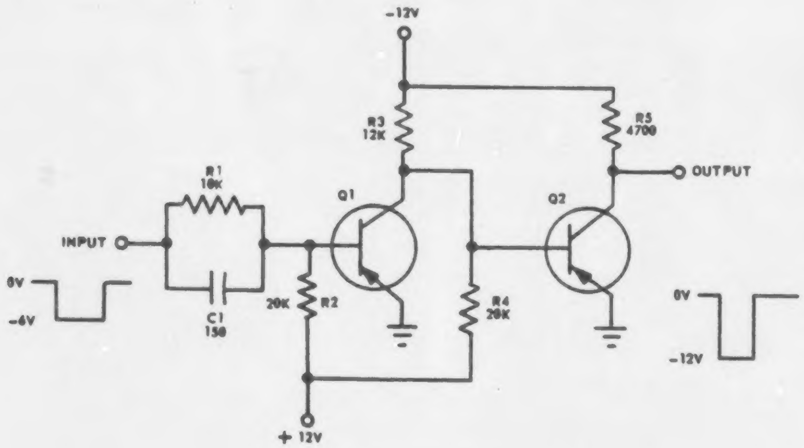


Fig 5-6. Level restorer.

When the input voltage changes to -6 volts, the input voltage divider--made up of R1 and R2--divides the input and source voltages so that a negative potential is felt on the base of Q1. This forward bias causes Q1 to conduct heavily. The collector voltage of Q1 goes to approximately ground potential, or 0 volts. Since this voltage is coupled to the base of Q2, Q2 almost ceases to conduct. Under these conditions, the collector of Q2 is about -12 volts. The input pulse of -6 volts is restored to the desired level of -12 volts in the output of this circui .

5-6. DELAY LINES

a. Delay lines are nonlogic circuits used to delay a signal input for a specific period. Delay lines made of inductors and capacitors (LC) are used to delay the signal from a few nanoseconds to as many as several hundred nanoseconds. Although delay times of several hundred microseconds are obtainable with LC delay lines, the large physical size of the components makes them impractical in digital equipment. In this case, mercury or magnetostrictive delay lines are used. Here we discuss only the LC type.

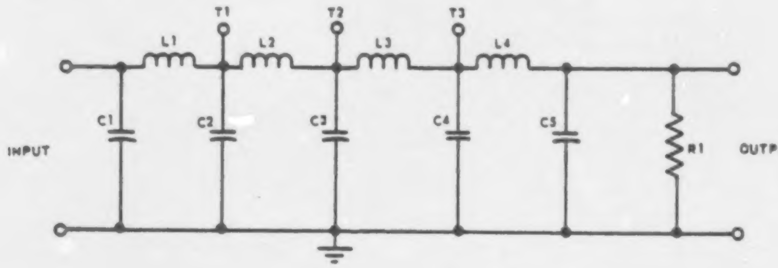


Fig 5-7. LC delay line.

b. Figure 5-7 shows a delay line that consists of a series of LC filter sections. A pulse applied to the input of the delay line charges C1 in a finite period of time. The voltage developed across C1 causes current flow through L1, which charges C2. This process continues with L2 and C3, L3 and C4, L4 and C5. Finally, C5's charging produces a voltage pulse across resistor R1. This output pulse appears at a fixed time after the pulse is applied to the input. The time difference between these pulses (the delay) is determined by the values of L and C and the number of LC sections. The equation used to compute the amount of delay time is:

$$T_0 = N \sqrt{LC}$$

T_0 is the time delay in seconds, N is the number of sections, L is the inductance in henrys per section, and C is the capacitance per section in farads. When a delay smaller than the total of the line is needed, the delay line may be tapped at one of the LC sections.

c. Symbols for time delay lines are shown in figure 5-8.

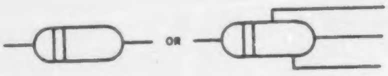


Fig 5-8. Symbols for delay lines.

5-7. SCHMITT TRIGGER CIRCUIT

a. When the quality of a signal has degenerated, the Schmitt trigger circuit is used to furnish a sharp rectangular output pulse of approximately the same duration and phase as the input pulse; thus it improves the pulse waveshape. It is also used to change a sine wave to a rectangular wave.

b. Figure 5-9 shows a Schmitt trigger circuit consisting of two common-emitter amplifiers, Q1 and Q2, and associated components.

c. In the quiescent state the input is at 0 volts or above trigger level, and Q1 is cut off. The voltage divider of R3, R4, and R5 divides the source voltages -12 volts and +12 volts so that the base of Q2 has a negative voltage applied. This forward bias causes Q2 to be operating at saturation. The current through Q2 causes the voltage drop across common emitter resistor R7 to reverse-bias Q1 and keep it at cutoff. In this condition, the output taken from the collector of Q2 is about 0 volts.

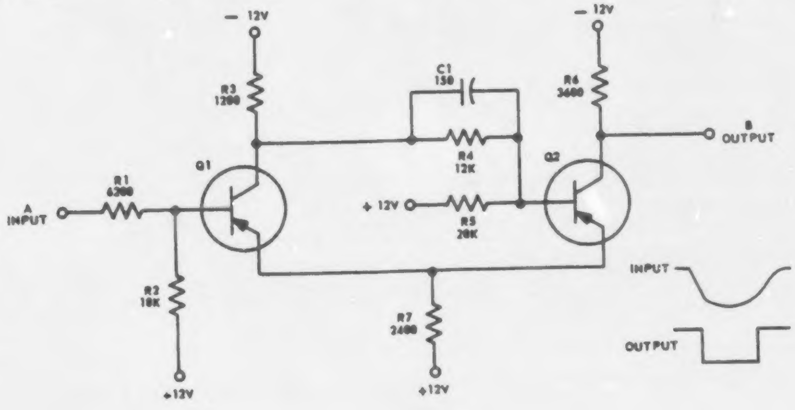


Fig 5-9. Schmitt trigger circuit.

d. When a negative voltage of sufficient amplitude is at the input, Q1 conducts and its collector goes toward 0 volts. This change is coupled to the base of Q2 and causes a decrease in the conduction of Q2. The decrease in current through R7 puts less reverse bias on the emitter of Q1 and causes Q1 to conduct more, making its collector become more positive and causing Q2 to conduct less. This action continues until Q1 is conducting at or near saturation, and Q2 is cut off by the collector potential of Q1. The collector voltage of Q2 is now –12 volts.

The circuit remains in this state until the input voltage decreases to below the level required to maintain the current flow at or near saturation. At this time, the collector potential of Q1 starts in the negative direction. This change is felt on the base of Q2 and starts Q2 conducting. Q2 conducting causes more current through R7, which puts reverse bias on Q1 and causes it to conduct less. Furthermore, it causes the Q2 collector to become more negative. This negative voltage causes Q2 to conduct more, and the action continues until Q1 is at cutoff and Q2 at saturation. The output is now near 0 volts.

The sharp rise and fall at the output is due to the rapid regeneration between Q1 and Q2. The purpose of C1 is to speed up this feedback.

e. The symbol for a Schmitt trigger circuit is a square labeled ST.

5-8. SINGLE-SHOT MULTIVIBRATOR

a. The monostable multivibrator, also called the single-shot multivibrator, is used for pulse stretching, pulse shaping, gate operating, and for providing delayed pulses.

b. Figure 5-10 shows a single-shot multivibrator and its waveshapes. In its quiescent state, Q3 conducts and Q2 is cut off. Q1 is a switching transistor, and it conducts only when an input pulse is applied. Prior to time T_0, the multivibrator is in the quiescent state, and the collector of Q3 is about -0.3 volt. This is sufficient to keep Q2 cut off. The collector of Q2 is at a negative Vcc.

At time T_0, a negative pulse is applied to the base of Q1; Q1 inverts this signal, and the positive pulse is coupled by C1 to the base of Q3 and drives Q3 to cutoff. The collector of Q3 starts going negative. This negative-going signal, V_{c3}, is directly coupled to the base of Q2, and Q2 starts to conduct. Q2 will then conduct as long as Q3 remains cut off. As Q2 conducts, its collector voltage becomes less negative. When this happens, there is nothing to keep the charge on C1. So C1 discharges from collector to emitter of Q2, through the power source (V_{cc} and then through R3 and R4 to the other plate of C1.

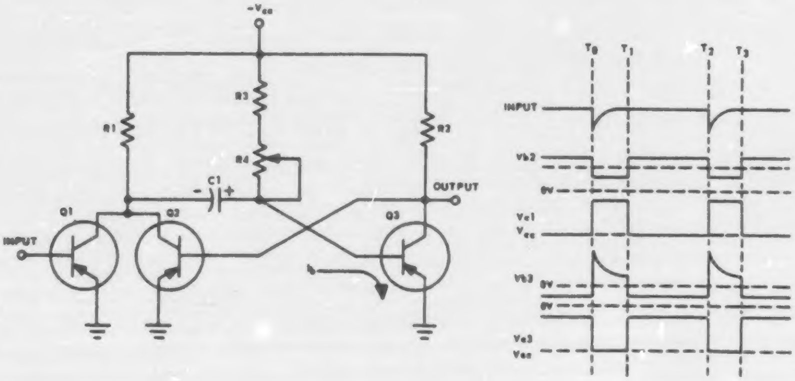


Fig 5-10. Single-shot multivibrator.

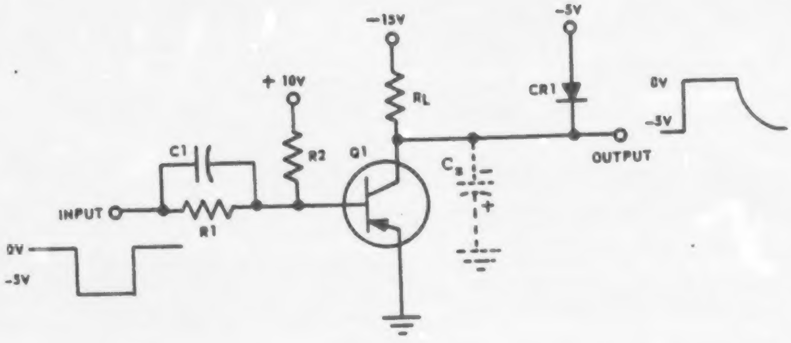
The voltage drop across R3 and R4, due to C1 discharging, keeps Q3 cut off until C1 discharges to the [illegible]e of Q3. Referring to the waveshapes in figure 5-11, notice that the base voltage of Q3, [illegible] follows the discharge of C1 between times T_0 and T_1. Since this voltage determines how long Q3 is cut off, the discharge time determines the width of the output pulse. At time T_1, Q3 starts to conduct and the collector voltage of Q3 starts to go less negative. This drives Q2 toward cutoff, and C1 is charged again by the I_b of Q3. The multivibrator is now back in the quiescent condition and ready to receive the next trigger. The output may be taken from either collector. The width of the output pulse is determined by the values of R3 and R4, since these values determine the discharge time of C1.

c. The symbol for a single-shot multivibrator is a square labeled SS.

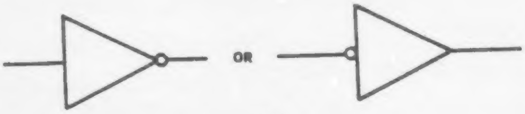
5-9. INVERTER

a. The inverter is a circuit which gives an output voltage 180° out of phase with the input voltage; it also gives high voltage and power gain. Inversion of a signal is the natural function of a common-emitter amplifier and a common-base amplifier. Inverters used in digital equipment are usually common-emitter amplifiers, because their configuration has the largest power gain, and a voltage gain as well as a current gain.

b. Figure 5-11A shows a basic inverter circuit which uses the grounded-emitter configuration. With the input voltage at a 0-volt level, the base of Q1 is at about +0.2 volt due to the ratio of resistors R1 and R2. This reverse bias is enough to cut off Q1. With no current flow through the transistor, its collector potential goes toward -15 volts. However, as soon as the collector voltage goes below -5 volts, CR1 conducts and limits the output to -5 volts.



A. CIRCUIT



B. SYMBOLS

Fig 5-11. Inverter.

When the input voltage drops to -5 volts, capacitor C1 couples the instantaneous change to the base of Q1 and causes it to conduct. The transistor operates at or near saturation. This causes the collector potential to rise to approximately 0 volts, which is the output voltage when the input is -5 volts. The transistor conducts as long as the input voltage is at -5 volts, but when the input returns to 0 volts, the transistor cuts off and the output returns to -5 volts.

c. Notice that the output voltage has a sharp rise time and a not-so-sharp fall time. --Let us see why this happens. --The stray capacitance, C_s, charges to -5 volts while the transistor is off. The path for the charge is from the -15 volts, to C_s, to ground, and back to the supply.

When the input changes from 0 volts to -5 volts, Q1 conducts. This provides a quick discharge path for C_s and gives a sharp rise time. When the input changes from -5 volts to 0 volts, Q2 cuts off. C_s now charges through R_L. This takes a longer time, resulting in the slow output fall time.

d. The symbols for the inverter are shown in figure 5-11B. As in logic circuits, the small circle, or state indicator, placed at the input means that the circuit is activated by a relatively low voltage. The small circle placed at the output means that the activated output is a relatively low voltage. The absence of the small circle, or state indicator, means that the circuit is activated by a relatively high voltage.

e. The inverter may be used to perform a logic function. Since the output is out of phase with the input, the inverter may be used to perform the NOT function.

5-10. SUMMARY

Digital equipment requires circuits other than logic circuits to perform efficiently and reliably.

a. The emitter-follower is used to match impedances; also as a current source.

b. The pulse amplifier is used to increase the amplitude of a pulse, to narrow a pulse width, and to increase the driving capabilities of a pulse.

c. The relay driver activates a relay coil.

d. The level restorer restores pulse voltages to the desired level.

e. Delay lines are used to delay a signal for a specified period. LC delay lines are used for delay times of a few nanoseconds through several hundred nanoseconds.

f. The Schmitt trigger furnishes a sharp rectangular output pulse from an input of distorted pulses or sinusoidal pulses.

g. The single-shot multivibrator produces gating pulses, increases or decreases pulse widths, and provides time delay between circuit actions.

h. The inverter provides phase inversion for pulses, and it is capable of furnishing high voltage and power gain.

Chapter 6

MAGNETIC CORES

6-1. INTRODUCTION

Certain magnetic alloys and ferrites remain magnetized for relatively long periods of time, and yet they can be easily demagnetized or remagnetized in the opposite direction when conditions warrant. The magnetic core has played a prominent role as a memory element in the development of large-scale digital equipment. In keeping with the miniaturization trend, the magnetic core has been made smaller through the development of new ferrite materials and fabricating techniques. Magnetic-core storage is the most widely used form of magnetic storage in present-day equipment.

In addition to miniaturization, the magnetic-core storage system offers other advantages, such as absence of moving parts and almost instantaneous access time. Like all magnetic storage devices, the magnetic core has the capability to store information indefinitely. However, unlike other forms of magnetic storage, information in the core is destroyed upon readout; therefore additional circuits are required to re-write the information back into the memory at the same time it is supplied to the required circuits.

6-2. HYSTERESIS LOOP

a. The basic principles of magnetic-core storage of binary information can be better understood through explanation of the hysteresis loop. Figure 6-1 represents an idealized B-H curve. Assume that the magnetic material has no previous magnetic history, a condition represented by point O. A magnetizing force H is applied. The magnetic flux density B will increase at a rate indicated by the dotted line. At the point marked R, the material becomes saturated; that is, an increase in the value of H beyond this point produces no further increase in B. When H is returned to zero, magnetic induction B_1 is retained within the material. The magnetizing force must be made equal to -H before the flux density becomes zero. When it is made more negative than -H, the material becomes saturated at point U. When -H is returned to zero, magnetic induction $-B_1$ will be retained within the material.

The path RSUVR represents the locus of the B-H curve as the ideal material is saturated in one direction, demagnetized, saturated in the opposite direction, and finally returned to the initial point of saturation. The inclosed area represents the work done in orienting the magnetic dipoles within the material. This loop is the hysteresis loop for the material.

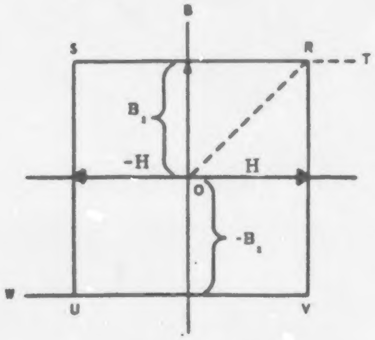


Fig 6-1. Idealized B-H curve.

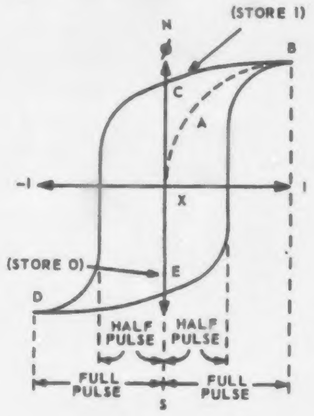


Fig 6-2. Hysteresis loop for a magnetic core.

b. Figure 6-2 represents a typical hysteresis loop for a magnetic core. In this figure, the B-axis is labeled ϕ and the H-axis is labeled I, since flux and current are the major factors which make up flux density and magnetizing force. The dotted line XAB indicates the initial path taken by the magnetic flux when an unmagnetized core has current applied for the first time. With enough current applied, the core will reach saturation at point B in the indicated N direction. If the current is removed, a slight decrease in magnetism occurs and causes the magnetic flux point to move from B to C, where it is held by residual magnetism.

c. Remember that a pulse of current which is capable of saturating the core in any one direction is known as a full pulse, and that a pulse of current extending only to the knee of the curve is known as a half pulse, as illustrated in figure 6-2. If the core is magnetized in the N direction (refer to point C on the curve), then a full-current pulse passed through the core in the opposite direction will cause the magnetic flux to traverse around the knee of the loop and down to point D, which corresponds to saturation in the S direction. When the pulse is removed, the magnetic flux point of the loop will change to E, which represents the residual magnetism. From this point, if the magnetism is reversed (switched) by a full pulse, the change in flux will follow the path EB. When reversed again by a full pulse, it will follow path CD.

d. From this discussion of the hysteresis loop, you can see that the core may be magnetized in either of two directions. This makes it an excellent bistable device for storing binary 1 and binary 0. Also, the squareness of the hysteresis loop shows that the magnetic field within the core may be reversed in a very short time.

e. There are two main types of magnetic cores: the metallic ribbon core and the ferrite core. The metallic-ribbon type is much larger than the ferrite core. It is used in shift registers, logic circuits, and storage registers. Ferrite cores are used in fast-access coincident current memory systems.

6-3. METALLIC RIBBON CORE

a. Construction. This type core is constructed by spirally winding a thin (1/8- to 1-mil gage) narrow molybdenum permalloy ribbon on a ceramic bobbin. The end of the tape is then spot-welded; the core is annealed and inserted in a plastic sleeve. The input winding, transfer winding, and output winding are then wound on this core. The core is ready to use as it is or, if necessary, it may be encased in a shockproof capsule. (Figure 6-3 shows the parts used in the construction of a metallic ribbon core.) The diameter of these cores ranges from 1/4 inch to 1/2 inch.

Note: Through common usage the metallic ribbon has come to be called a bimagnetic or bimag core.

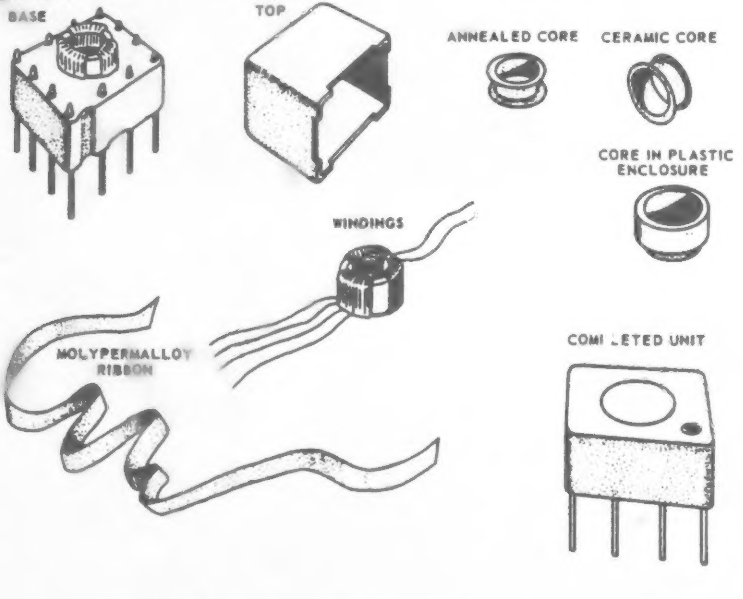


Fig 6-3. Parts of a metallic ribbon core.

b. Dot notation. Figure 6-4 illustrates the schematic of a metallic ribbon core with dot notation that reduces the confusion involved in relating the voltages and currents present in the windings of a core. These conventions are important:

(1) Electron current entering the nondot side of a winding tends to switch the core to the ZERO state.

(2) Electron current entering the dot side of a winding tends to switch the core to the ONE state.

(3) When a core switches to the ZERO state, the polarity at the dot side of the output winding is positive.

For example, assume that the core in figure 6-4 is in the ZERO state and current enters the dot terminal of winding L1. A large flux variation takes place, and a large voltage is induced across winding L2. The dot terminal is then negative, and the nondot terminal is positive. Since L2 is comparable to a secondary, and a secondary acts as a power source, current flows from the dot terminal of L2.

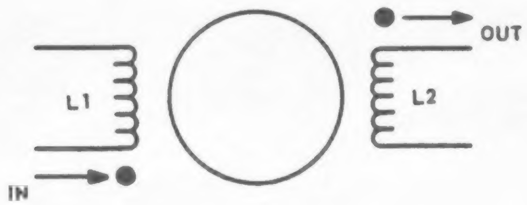


Fig 6-4. Metallic ribbon core symbol.

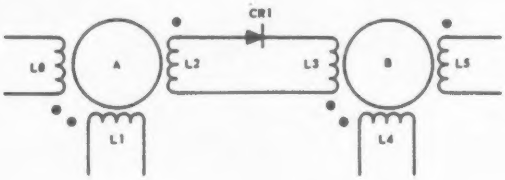


Fig 6-5. Single-diode transfer loop.

c. Single-diode transfer loop. Although the core can store data for an indefinite period, to be useful the data must be transferred from one core to another or to some associated circuit. The transfer loop does this. The most frequently used transfer loop is the single-diode (fig 6-5) and associated windings.

(1) For explanation, let us assume that core A in figure 6-5 is in the ZERO state. When a data pulse which represents a binary 1 is applied to winding L0, it causes current to flow into the dot side of winding L0. A large flux variation takes place and the core is switched to the ONE state. The output winding L2 has a voltage induced, but no current can flow from it to winding L3, due to the high back resistance of CR1. Next, a transfer pulse is applied to L1. Current flows into the nondot side of the winding L1 and switches core A to the ZERO state. During this switching action a large flux variation takes place, and a voltage is induced in the output winding L2. The dot terminal of L2 is positive and the nondot terminal is negative. The output winding acts as a power source and causes current to flow into the dot terminal of winding L3, through winding L3, through the low forward resistance of CR1, and back to the dot terminal of L2. This switches core B to the ONE state. Core A is now in the ZERO state, and binary 1 has been transferred from core A to core B. To transfer the binary 1 from core B to another core or associated circuit, a transfer pulse would have to be applied to winding L4.

(2) The only flux changes in core A that should be felt in core B are those caused by switching core A from the ONE state to the ZERO state. Any other change is undesirable. For example, core A is in the ZERO state, core B is in the ONE state. Then, if a data pulse representing a binary 1 is applied to winding L0, core A will go to the ONE state. When this happens, a voltage is induced in output winding L2 with the dot terminal negative and the nondot terminal positive. Without CR1, current would flow into nondot terminal of L3 and prematurely switch core B to the ZERO state. Obviously this is undesirable. So CR1 is added and current can flow in one direction only; that is, into the dot terminal of L3. Thus, the function of the crystal diode in the single-diode loop is to prevent premature switching of the receiving core.

(3) Another problem is reverse transfer; that is, the transfer of a binary 1 from core B to core A when a transfer pulse is applied to L4. For example, assume that core A is in the ZERO state and core B is in the ONE state. A transfer pulse is applied to L4, and current flows into the nondot side. A large flux variation occurs and switches core B to the ZERO state. Positive polarities occur at the dot terminals of L3 and L5, and negative polarities occur at the nondot terminals. Both L3 and L5 are acting as secondaries of a transformer and therefore as power sources. This is desired in L5 as was explained, but in L3 it presents a problem. Current flow out of the nondot terminal of L3 through CR1 into the dot terminal would switch core A to the ONE state. To keep this from happening, the output winding L2 has three to five times as many turns as the input winding L3. The output winding offers a high impedance to this undesired current, and keeps it down to a non-switching level.

d. Analysis.

(1) The next input pulse occurring at time T_0 causes the current to flow into the dot side of the input winding. There is a large flux variation to point B (positive saturation on the hysteresis loop in fig 6-2), and consequently an induced output signal. At time T_1, when the input current goes back to zero, the flux drops to point C. This flux is the residual magnetism, and the core now contains a binary 1.

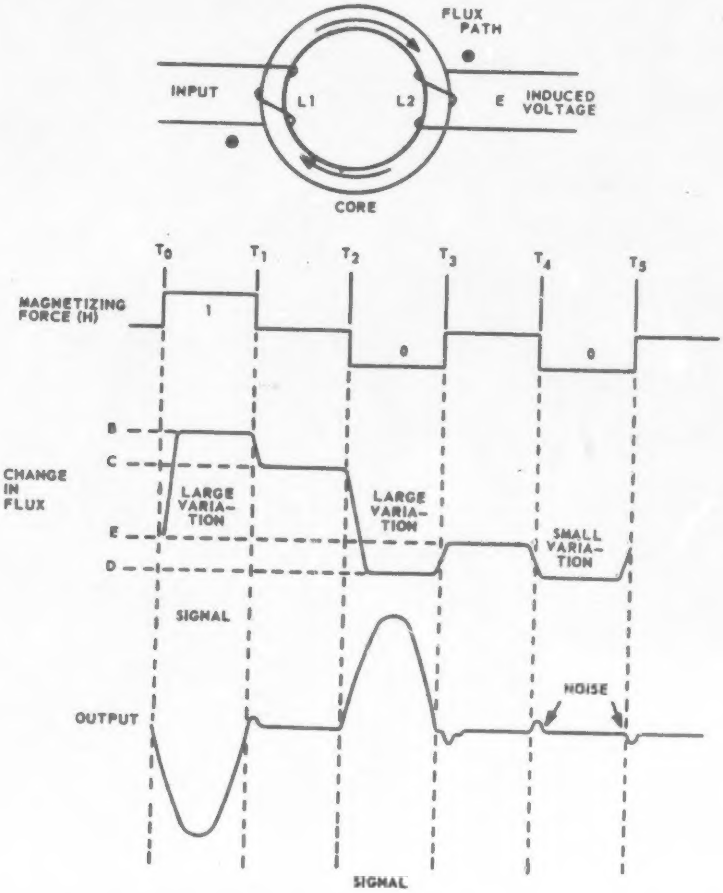

FLUX PATH
INPUT
L1
L2
E
INDUCED VOLTAGE
CORE
T_0
T_1
T_2
T_3
T_4
T_5
MAGNETIZING FORCE (H)
1
0
0
B
C
E
D
CHANGE IN FLUX
LARGE VARIATION
LARGE VARIATION
SMALL VARIATION
SIGNAL
OUTPUT
NOISE
SIGNAL

Fig 6-6. Metallic ribbon core and waveshapes.

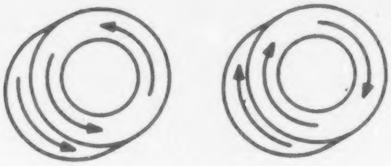
(2) At time T_2, an input pulse causes current to flow into the nondot side of the input winding. There is a large flux variation to D (negative saturation on the hysteresis loop), and consequently an induced output signal. At time T_3, when the input signal goes back to zero, the flux decreases to point E. This flux is the residual magnetism. The core now contains a binary 0.

(3) Assume that at time T_4 another pulse is applied with the proper polarity to store a binary 0. In this case, the core already contains a binary 0, so the flux variation is small from E to D. This small variation induces small voltages (called noise) in the output winding. They are too small to activate the circuits connected to the output winding.

6-4. FERRITE CORE

a. Construction. The ferrite core is a small toroid made of a brittle, ceramic-type material whose ingredients are iron oxide, manganese, nonmetallic oxides, and an organic binder. Although not all of these materials are in themselves magnetic, the finished core exhibits strong ferromagnetic characteristics when the substances are mixed, formed, heated in a kiln, and cooled. Kiln temperature and length of baking time determine the properties of the ferrite, and a variation of as little as 1% can cause a complete change in core characteristics. Physically, the ferrite core is a small ring (similar to a doughnut or a toroid) with an approximate inner diameter of 0.050 inch and an outer diameter of 0.080 inch. They are used extensively in magnetic storage systems.

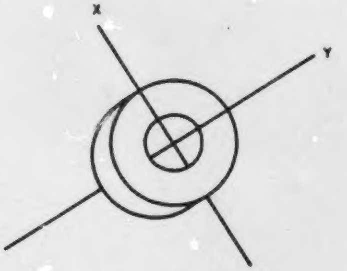
b. Functions. How does the ferrite core store binary information? In the hysteresis loop (fig 6-2), we saw that a core may be magnetized in either of two directions. We say that the core is storing 1 or is in the ONE state when the magnetism is at point C on the curve, and that it is storing 0 or is in the ZERO state when the magnetism is at point E. These conditions could be reversed if desired, but for our explanation we use the conditions stated. Figure 6-7A shows the direction of the flux in a core storing 1, and B shows the direction of the flux in a core storing 0.



A. STORING 1 B. STORING 0

Fig 6-7. Ferrite cores.

To change the state of either core, the magnetic field in the core is reversed. --In the hysteresis loop (fig 6-2), we noted that the state could be changed by using one full-current pulse or two half-current pulses applied simultaneously. The transfer is accomplished by two drive wires passed through the center of the core (fig 6-8). For convenience, the drive wires are designated as X and Y; sometimes they are labeled the X address and the Y address. To write into a core or to read out of a core, each drive wire must supply half the current necessary to produce a full-current pulse. To switch the magnetism of a core, both X and Y wires must be energized simultaneously to supply a field large enough to reverse the magnetization of the core. Thus, the phrase describing the common type of storage system employing ferrite cores is the coincident current memory arrangement. Two additional windings are usually employed: one for sense (reading) and one for inhibit (fig 6-9).



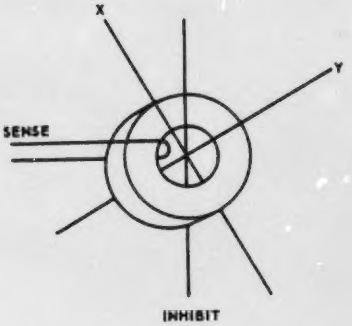
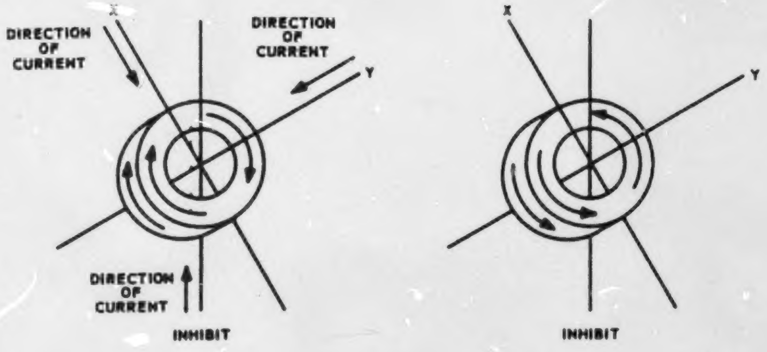


Fig 6-8. Drive wires of core.

Fig 6-9. Wiring of typical memory core.

To understand how the write function takes place, assume that the core in figure 6-10A is in the ZERO state and magnetized in the direction shown. A half-current pulse is applied to the X drive wire in the direction shown; at the same time, another half-current pulse is applied to the Y drive wire as in figure 6-10A. No current is applied to the inhibit wire at this time. Coincidence of the currents takes place in the center of the core. The field produced by this equivalent full-current pulse switches the magnetic field to the direction shown in figure 6-10B. The core now is storing a binary 1. Since all the cores on these X and Y drive wires are pulsed at the same time, you may wonder how binary 0's are permitted to remain in the cores which are to store 0's. --The inhibit wire of the core which is to store 0 is used when 0 is to be written. A half-current pulse passes through this wire simultaneously with the currents through the X and Y wires. The direction of the inhibit current is opposite to the X and Y currents, as in figure 6-10A. Since the current is in an opposite direction, the field produced by it cancels half of the field of the X and Y currents. Therefore, the magnetic field, since it is too small to switch the core to the other state, remains in the direction shown in figure 6-10A. The core now continues storing a binary 0.



A. ZERO STATE

B. ONE STATE

Fig 6-10. Writing into a ferrite core.

To read from a core, the sense wire and the X and Y drive wires are used. Figure 6-11A shows a core in the ONE state. As in the store function, half-current pulses are applied to the X and Y drive wires simultaneously. However, notice that in figure 6-11A the direction of current for reading is opposite the direction of current during writing, as the arrows show. The half-current pulses add in the center of the core to equal a full-current pulse. The resultant magnetic field is large enough to switch the flux in the core to the opposite direction (fig 6-11B). The large change in magnetic flux induces a voltage in the sense wire. This pulse represents a binary 1. It is amplified and shaped to be used in other circuits. If the core had been in the ZERO state (as in fig 6-11B), current flow in the X and Y wires in the direction shown in figure 6-11A would not change the direction of the magnetic field. Thus, no voltage would be induced in the sense wire.

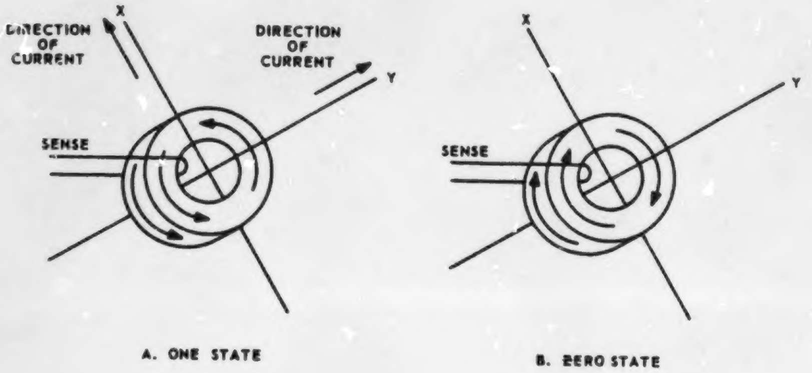


Fig 6-11. Reading from a ferrite core.

Since the core that stores 1 switches to the ZERO state upon each readout, the readout is said to be destructive. To be retained, the data must be rewritten into the core after each readout. This requires extra circuitry and decreases the access time of the memory unit.

To store large or small quantities of binary information, the ferrite cores must be so arranged as to provide efficient access to specific bits. The cores may be assembled into planes or matrices. Figure 6-12 illustrates a simple 4 X 4 core plane with a storage capacity of 16 information bits. To address any core in the plane, a half pulse is passed in the read direction on one X coordinate and on one Y coordinate. Such pulses add so that the core at the point of intersection receives a full-current pulse. In the case shown in figure 6-12, half pulses applied to Y coordinate 2 and X coordinate 2 result in a full pulse at the dark-shaded core. All other cores on the respective X and Y lines (indicated by light shading) are subjected to half pulses. The application of a half pulse does not change the state of any of these cores.

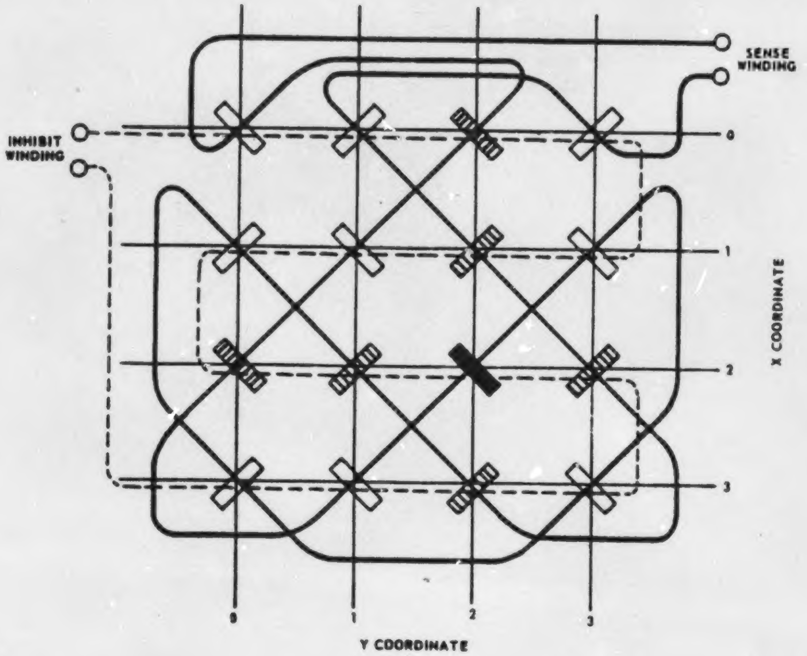
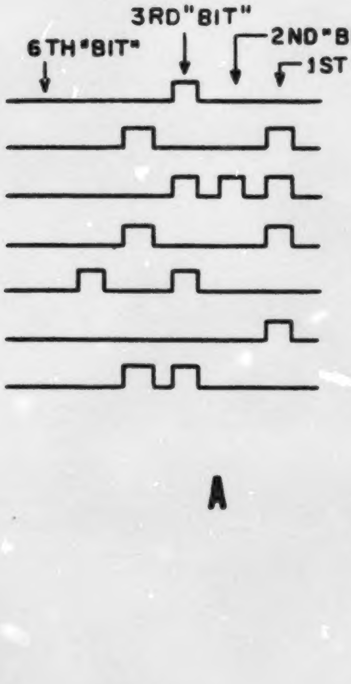

SENSE WINDING
INHIBIT WINDING
0
1
2
3
X COORDINATE
0
1
2
3
Y COORDINATE

Fig 6-12. Ferrite core matrix.

The information to be stored normally consists of a series of information bits which make up a binary word. Each binary word may represent a single character of the alphabet or several characters depending on the capacity of the computer. Figure 6-13A illustrates the word DIGITAL in binary form. A portion of the code used is shown in figure 6-13B.

NOTE

PULSE =1
NO PULSE=0


3RD"BIT"
6TH"BIT"
2ND"BIT"
1ST"BIT"

0 0 0 1 0 0 = D
0 0 1 0 0 1 = I
0 0 0 1 1 1 = G
0 0 1 0 0 1 = I
0 1 0 1 0 0 = T
0 0 0 0 0 1 = A
0 0 1 1 0 0 = L

A

CODE

CHARACTER	BINARY FORM
A	0 0 0 0 0 1
B	0 0 0 0 1 0
C	0 0 0 0 1 1
D	0 0 0 1 0 0
ETC.	ETC.
.	
,	

B

Fig 6-13. Binary words.

In order to store larger quantities of binary information, ferrite cores are assembled into planes or matrices whose size is determined by the number of words or units of information the memory is required to store.

Once the size of the matrix has been determined (usually some power of 2), only the number of digits per word remains to be selected. Since each core of a plane represents one digit of a word, the number of planes required will be equal to the number of digits per word. For example, a memory of 4 x 4 planes stacked four high would have a capacity of sixteen 4-digit words.

6-5. SUMMARY

Static magnetic storage is made possible by the use of ferrites and other materials which possess certain magnetic characteristics. Magnetic cores with their square hysteresis loops make possible high switching speeds.

a. The metallic ribbon core device is used mainly for storage and shift registers. This bimagnetic core stores the binary 1 or 0. Information is applied through an input winding and read out through an output winding. Transfer between cores is accomplished by the use of transfer loops.

b. The ferrite core is used in coincident current memory units. The core discriminates against half-current pulses and switches on full-current pulses. Thus, addressing a set of cores in the core planes is easily accomplished by applying a half-current pulse on one coordinate and a half-current pulse on the other coordinate. The core of each plane at the intersection of the coordinates receives a full-current pulse which interrogates the core in reading. If the core contains 1, it will switch to the 0 state and induce an output on the sense wire for that plane. To write back in, the same set of coordinates is current-pulsed in the opposite direction, which will put 1 in the core of every plane. If it is desired to leave a 0 in the core of a particular plane, the inhibit driver for that plane must be turned on. The current from the inhibit driver opposes one of the coordinate half-current pulses and cancels it. Thus, the core for that plane does not receive a full current pulse and will not switch to the 1 state.

Chapter 7

LOGIC CIRCUITS

7-1. INTRODUCTION

a. The basic funtions of digital equipment are to count, store, compare, and transfer information during a controlled time interval. Logical functions of these machines depend primarily upon the action of counters, registers, decoders, and encoders that are formed by combinations of logic switching circuits and flip-flops.

b. In prior chapters, we have studied circuits that are used as fundamental building blocks. Now we put these blocks together to perform logical operations. In this chapter, we discuss serial and parallel counters, storage and shift registers, decoders, and encoders.

7-2. COUNTERS

A counter is any device which can count, record, and indicate input information in a sequential manner. In logic machines, a counter may serve many seemingly unrelated purposes. Although its basic function is to count, the counter output may be used to form a gating voltage or a trigger for another logic circuit; also to reset the counter and begin a new counting operation.

When classified according to circuit design, counters are either serial or parallel. When classified according to function, counters are up-counters, down-counters, or a combination of the two. Up-counters count or add the number of input pulses. Down-counters subtract the input count or count down from some preset number.

Counters are often made up of several logic flip-flops connected together in series or in parallel so as to count input pulses. The states of the flip-flops indicate the count in the counter.

a. Serial up-counter. A serial up-counter consists of a group of flip-flops that counts a series of pulses that may or may not be periodic. The flip-flops are so connected that each will change from the ZERO to the ONE state, or conversely, as it receives the pulse of the output voltage from the preceding flip-flop or other triggering circuit. The construction of the flip-flops used in the counters will determine whether the leading or lagging edge of the pulse triggers the flip-flop. The serial counter is used to count sequentially all pulses presented to the input. Each pulse applied to the counter input changes the state of one or more of the flip-flops so that the state of these flip-flops represents the number of pulses counted.

Note: The serial-up counter counts only negative or positive pulses depending upon the construction of the counter. It does not count the absence of a pulse and therefore is used to count continuous pulse trains rather than binary combinations.

In the basic 4-stage serial up-counter shown in figure 7-1, each flip-flop represents a power of 2 where $A = 2_0$, $B = 2_1$, $C = 2_2$, and $D = 2_3$. This counter has 16 different possible states and, with the application of each input pulse, the circuit will make a progressive transition from state to state. The 16th input pulse will reset the counter to its original state. These features can be recognized from the waveform chart in figure 7-1. The counting of the counter is closely associated with the binary system of representing numbers.

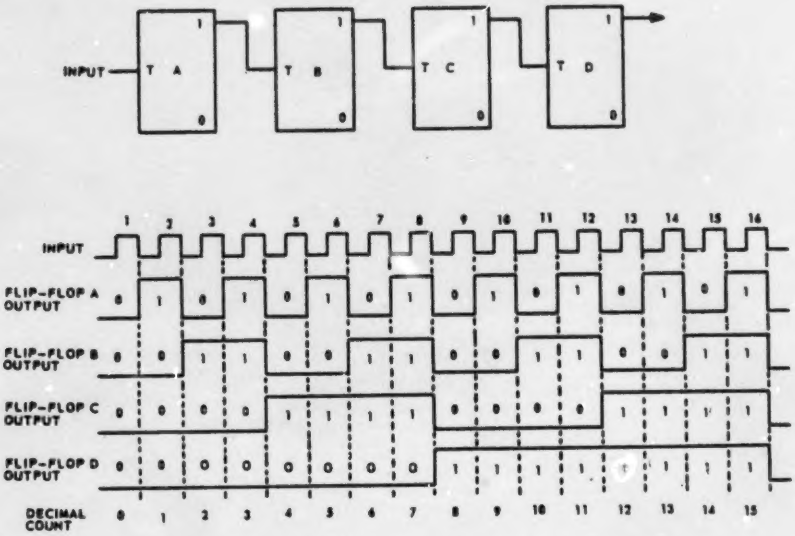

INPUT
T A
T B
T C
T D
1
0
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
INPUT
FLIP-FLOP A OUTPUT
FLIP-FLOP B OUTPUT
FLIP-FLOP C OUTPUT
FLIP-FLOP D OUTPUT
DECIMAL COUNT
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Fig 7-1. Serial up-counter.

Note: A short list of equivalent numbers in decimal and binary notations is given in table 7-1 for review.

Table 7-1. Equivalent Numbers in Decimal and Binary Notations

DECIMAL	BINARY	DECIMAL	BINARY
0	0 0 0 0	8	1 0 0 0
1	0 0 0 1	9	1 0 0 1
2	0 0 1 0	10	1 0 1 0
3	0 0 1 1	11	1 0 1 1
4	0 1 0 0	12	1 1 0 0
5	0 1 0 1	13	1 1 0 1
6	0 1 1 0	14	1 1 1 0
7	0 1 1 1	15	1 1 1 1

The output from each flip-flop in figure 7-1 is taken off the ONE side and fed to the complementing input of each succeeding flip-flop. Before the application of the first pulse, we assume that all the flip-flops are reset to the ZERO state; also, that the flip-flops are the complementing type and change states on the trailing edge of positive input pulses (negative-going voltages). The high-voltage level represents the binary 1.

If a negative-going pulse is applied to flip-flop A, it will cause a transition from the ZERO state to the ONE state, as can be seen by the waveforms in figure 7-1. Flip-flop A is now in the ONE state. Flip-flop B is not affected since it has felt a positive-going voltage from flip-flop A. The overall result is that flip-flop A has changed to the ONE state and all the other flip-flops remain in the ZERO state.

The second externally applied pulse causes flip-flop A to return from the ONE state to the ZERO state. Flip-flop B now receives a negative-going voltage and changes from the ZERO to the ONE state. Flip-flop C does not respond to the change in flip-flop B, since C receives a positive-going voltage. The overall result of the application of the second input pulse is that flip-flop B is in the ONE state while all the other flip-flops are in the ZERO state. From this we can see that: (1) flip-flop A makes a transition at each input pulse; and (2) each of the other flip-flops makes a transition when, and only when, the preceding flip-flop makes a transition from the ONE to the ZERO state.

Table 7-2. Number Representation in Serial Up-counter

NUMBER OF PULSES	FLIP-FLOPS				NUMBER OF PULSES	FLIP-FLOPS			
	A	B	C	D		A	B	C	D
0	0	0	0	0	8	0	0	0	1
1	1	0	0	0	9	1	0	0	1
2	0	1	0	0	10	0	1	0	1
3	1	1	0	0	11	1	1	0	1
4	0	0	1	0	12	0	0	1	1
5	1	0	1	0	13	1	0	1	1
6	0	1	1	0	14	0	1	1	1
7	1	1	1	0	15	1	1	1	1

Table 7-2 shows the resulting state of the flip-flops of the counter in figure 7-1 after a given number of input pulses. Compare this table with table 7-1. Note that the state of the flip-flops corresponds to the binary count of the number of input pulses. Thus, when 7 pulses have been received by the counter, flip-flops A, B, and C are in the ONE state and D is in the ZERO state (1110). The binary representation for 7 is 1110 (LSD on the left).

The maximum count of a serial counter may be extended by adding more flip-flops. To read the count of a serial counter, it is necessary to use neon lamps, a meter, or an oscilloscope to observe the individual flip-flops to determine the state that they have assumed.

b. Serial down-counter. A serial down-counter is designed to decrease its count by one with each input pulse. We have just discussed the serial up-counter, shown in figure 7-1. To change the circuit to a down-counter, the output from each flip-flop is taken from the ZERO side instead of the ONE side. Figure 7-2 shows how the flip-flops are connected to form a serial down-counter.

If a flip-flop makes the transition from the ZERO state to the ONE state, the ONE-side output is positive-going while the ZERO-side output is negative-going. The negative-going output from the ZERO-side will cause a transition in the flip-flop to which it is connected. Thus, the flip-flop will change states when the preceding flip-flop goes from the ZERO state to the ONE state.

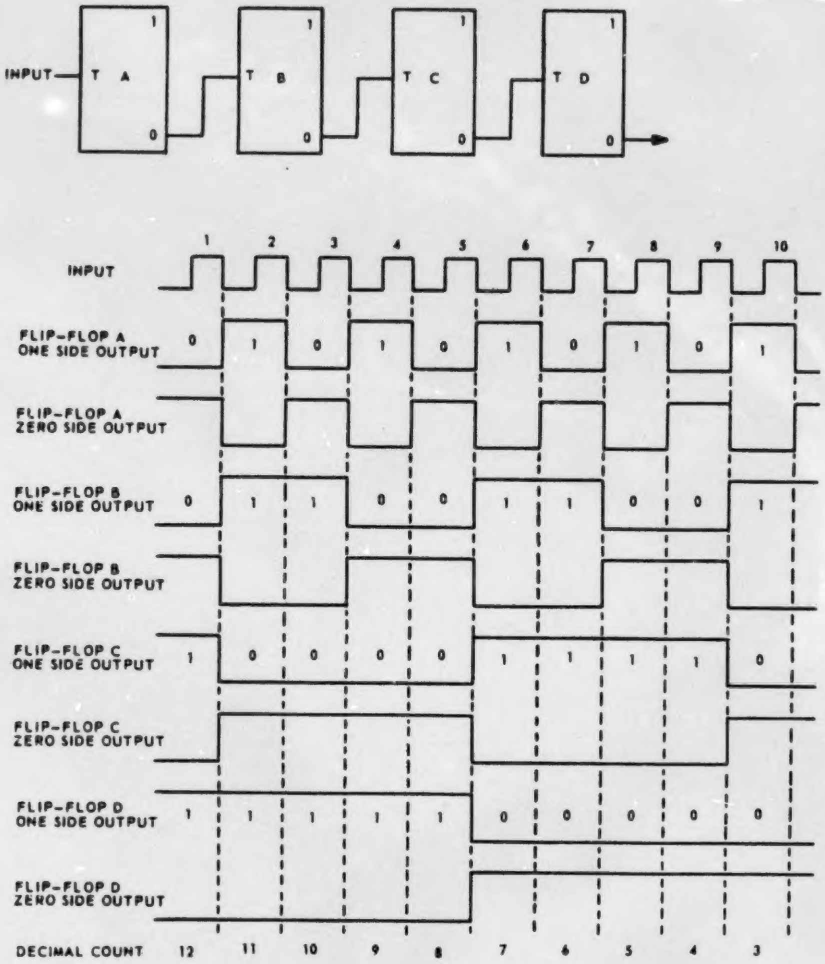

INPUT
T A
T B
T C
T D
1
0
INPUT
1 2 3 4 5 6 7 8 9 10
FLIP-FLOP A ONE SIDE OUTPUT
0 1 0 1 0 1 0 1 0 1
FLIP-FLOP A ZERO SIDE OUTPUT
FLIP-FLOP B ONE SIDE OUTPUT
0 1 1 0 0 1 1 0 0 1
FLIP-FLOP B ZERO SIDE OUTPUT
FLIP-FLOP C ONE SIDE OUTPUT
1 0 0 0 0 1 1 1 1 0
FLIP-FLOP C ZERO SIDE OUTPUT
FLIP-FLOP D ONE SIDE OUTPUT
1 1 1 1 1 0 0 0 0 0
FLIP-FLOP D ZERO SIDE OUTPUT
DECIMAL COUNT
12 11 10 9 8 7 6 5 4 3

Fig 7-2. Serial down-counter.

Consider the counter in figure 7-2 as having a binary count of 1100, which, of course, equals decimal 12. From the waveshapes you see that flip-flops A and B are in the ZERO state and flips-flops C and D are in the ONE state prior to the input pulse number 1. As input pulse number 1 goes negative, flip-flop A goes to the ONE state. This change of state causes flip-flop B to change from the ZERO state to the ONE state. This change of state causes flip-flop C to change from the ONE state to the ZERO state. The transition of flip-flop C does not affect flip-flop D; thus, flip-flop D remains in the ONE state. The result is that the counter now contains a binary count of 1011, which is decimal 11. Since the original number was 12, it is obvious that a subtraction of 1 has taken place.

> Note: Subtractors are very similar to adders. The purpose of a subtractor is to subtract one binary number from another in accordance with the rules for binary subtraction. This may be done through the addition of the complement as discussed in paragraph 1-7. Because of a great similarity between subtractors and adders, subtractors will not be discussed in detail.

c. Serial gated counter. The flip-flops used in the serial counters in figures 7-1 and 7-2 require a finite amount of time to change state. Although this time is small, it is a factor that cannot be ignored. In a serial counter, a flip-flop cannot change its state until the preceding stage has changed state. This means that the time required for a serial-counter flip-flop to change states is multiplied by the number of stages, to get the total time for the pulse to travel from the first stage to the last.

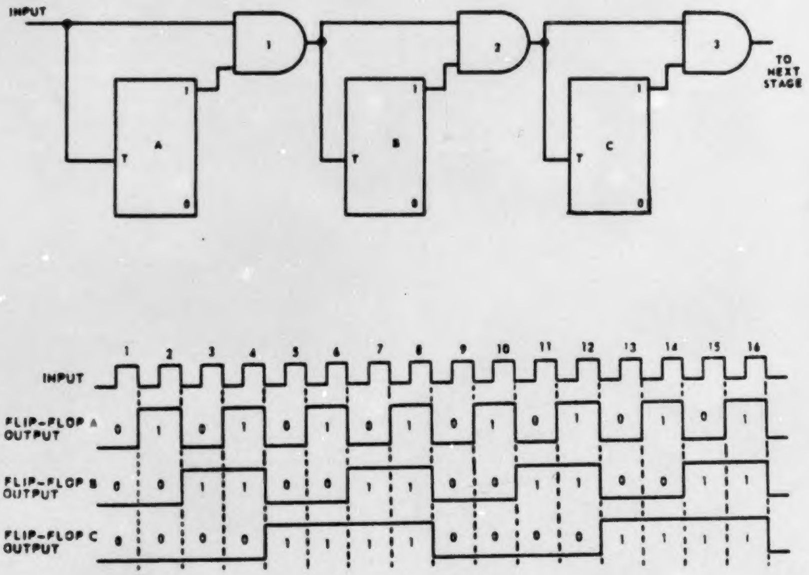


Fig 7-3. Serial up-counter with series gates.

The accumulative delay time can be made less by use of the circuit shown in figure 7-3. Notice that the input pulses are fed to AND gate 1 as well as the trigger input of flip-flop A. The other input to AND gate 1 is supplied by the ONE output of flip-flop A. If flip-flop A is in the ONE state when a input pulse is applied, the gate will be activated and supply an input pulse to flip-flop B and AND gate 2. Flip-flop B therefore receives a trigger input at the same time as flip-flop A, thereby eliminating the delay. If flip-flop A had been in the ZERO state, prior to the application of the input pulse, no output would have been present at the ONE side and gate 1 would not have passed the input pulse to flip-flop B. For example assume that the flip-flops will change state as the input pulses go in the negative direction and that a negative voltage is present at the ONE output when the flip-flops are in the ONE state and 0 volts are present at the ONE output when the flip-flops are in the ZERO state. Also assume that input pulse #6 is applied to the input.

Flip-flops A and C are in the ONE state and flip-flop B is in the ZERO state; therefore only AND gates 1 and 3 have negative voltages applied to input. When input pulse #6 goes negative the following action takes place: The negative-going voltage at the T input to flip-flop A causes it to change states. At the same time, the negative-going voltage is applied to AND gate 1. Since a negative voltage is already present at the other input, a negative output pulse is supplied to the T input of flip-flop B causing it to change states. Gate 1 also supplies a negative pulse to gate 2, but no action takes place because the other input is at 0 volts. Flip-flop C therefore has no input supplied and does not change states.

The counting in the counter in figure 7-3 is the same as that derived in figures 7-1 and 7-2. The counter in figure 7-3 has a faster speed because the gates are preconditioned so that changing the state of a flip-flop does not depend on the preceding flip-flop's change of states. However, the number of stages that can be used without amplification is limited, because the input pulse is attenuated by each gate, and may require restoration after several stages.

d. Parallel up-counter. As we have shown, serial counters with many stages have troublesome cumulative delay time. Such delay can cause problems especially when other circuits in the equipment must remain idle while waiting for the counter. Figure 7-4 is a parallel-type counter that reduces this delay problem but requires more gating circuitry.

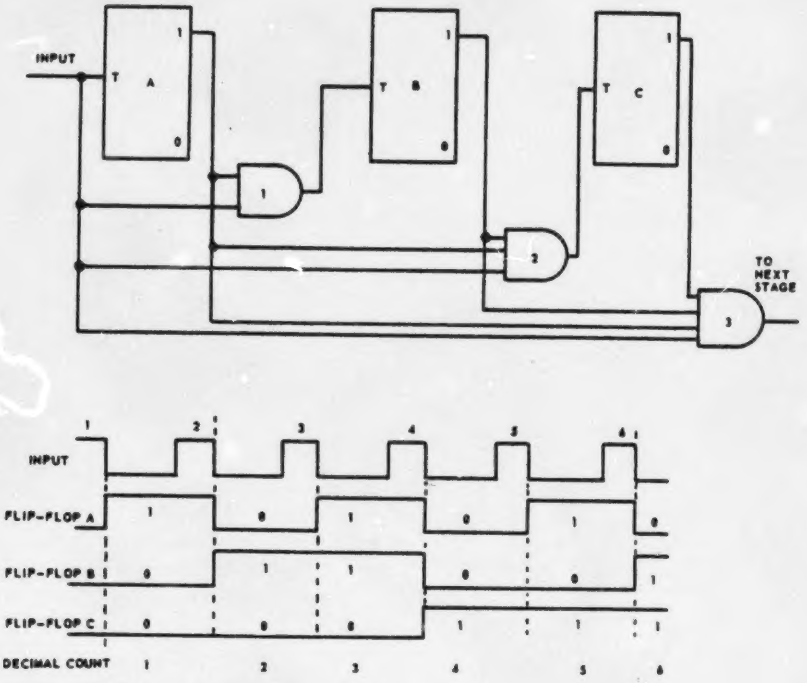


Fig 7-4. Parallel up-counter.

For discussion of the circuit in figure 7-4, let us assume that the flip-flops change states on the negative-going pulse and that a positive level of logic is used. Before the first input pulse is applied, all of the flip-flops are in the ZERO state.

The first input pulse is applied to the complement input of flip-flop A and to gates 1, 2, and 3. Gates 1, 2, and 3 have low inputs from the ONE sides of the flip-flops. Since all the flip-flops are in the ZERO state, the gates are not activated by the first input pulse. Therefore, flip-flops B and C remain in the ZERO state, while flip-flop A changes to the ONE state. The counter now contains a decimal count of 1, or binary 001, and gate 1 now has one high input from the ONE side of flip-flop A. Figure 7-4 shows the waveforms which cause the action of the flip-flops, and the binary and decimal count in the counter after each input pulse.

The second input pulse is applied to flip-flop A and gates 1, 2, and 3. Flip-flop A changes to the ZERO state. Since gate 1 is preconditioned with the high from the ONE side of flip-flop A, the input pulse activates gate 1 and changes flip-flop B to the ONE state. Gate 2 is not activated because of the low input from the ONE side of flip-flop B. Therefore, flip-flop C remains in the ZERO state. The counter now contains a count of 2 (010).

Gate 2 now has one high and one low input from flip-flops B and A, respectively. The third input pulse is applied to flip-flop A and gates 1, 2, and 3. Flip-flop A changes to the ONE state. None of the gates is activated by the pulse. Therefore, flip-flops B and C remain unchanged. The counter now contains a count of 3 (011).

Gate 1 now has one high input and gate 2 has two high inputs. The fourth input pulse is applied to flip-flop A and to gates 1, 2, and 3. Flip-flop A changes to the ZERO state. The input pulse activates gates 1 and 2, and changes flip-flop B to the ZERO state and flip-flop C to the ONE state. The counter now contains a count of 4 (100).

As the number of input pulses increases, the count in the counter will progress until a maximum count of 7 (111) is reached. The next pulse will set all the flip-flops to zero, and the count will start over.

To cause any flip-flop in a parallel counter to change states, all the preceding flip-flops must be in the ONE state. The waveforms for the parallel counter in figure 7-4 are the same as for the serial counter in figure 7-1. The speed of counting is the only difference. The time required to go from one count to the next is equal to the switching time of one flip-flop.

e. Parallel down-counter. The function of the parallel down-counter is the same as that of the serial down-counter. That is, the count in the counter decreases by one when an input pulse is applied. However, the parallel down-counter operates at a higher speed than the serial down-counter. Figure 7-5 shows a parallel down-counter and its waveforms. Notice that the difference between this counter and the one in figure 7-4 is that the output from the flip-flops is taken from the ZERO side instead of the ONE side. The operation of the two is similar; therefore, we shall not go through the operation again.

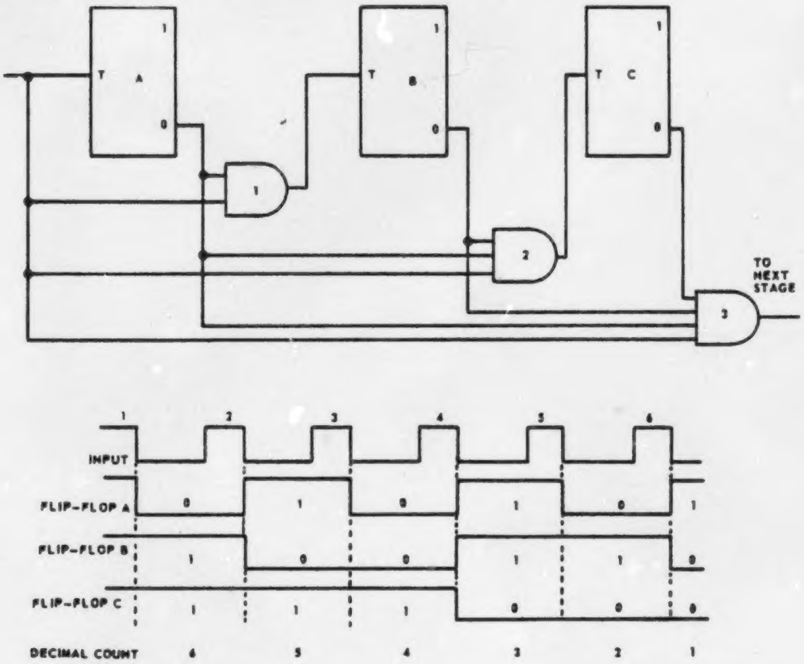


Fig 7-5. Parallel down-counter.

f. Decimal counter. A decimal counter counts 0 through 9. A 3-stage binary counter counts to a maximum of decimal 7. A 4-stage binary counter counts to a maximum of decimal 15. Therefore, to have a binary counter that counts to decimal 9, a 4-stage counter with modifications to remove the last six binary combinations must be used.

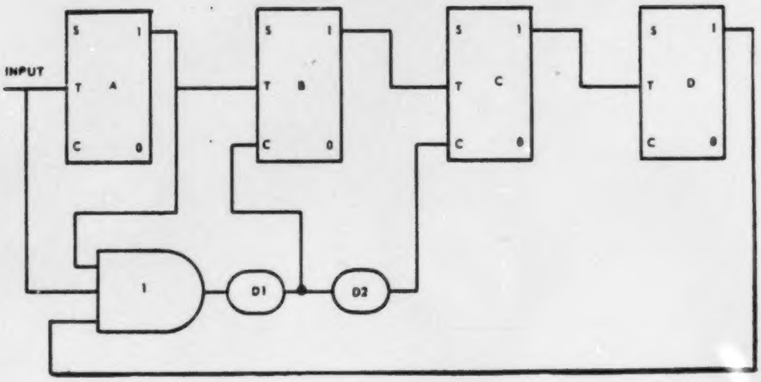


Fig 7-6. Decimal counter.

Figure 7-6 shows a counter that does this by using an AND gate and two delay lines. The counter is a serial-type up-counter that operates normally until it reaches a decimal count of 9 or binary 1001. With 1001 in the counter, gate 1 will have two activating signals from the ONE sides of flip-flops A and D. The next input pulse changes flip-flop A to the ZERO state. This change causes flip-flop B to flip to the ONE state. However, the input pulse also activates gate 1. The output of the gate goes through a delay line, D1, to the clear or reset side of flip-flop B. The delay allows the output of gate 1 to change flip-flop B to the ZERO state after the output of flip-flop A has flipped it to the ONE state. The change of flip-flop B from the ONE state to the ZERO state changes flip-flop C to the ONE state. The output of gate 1 is applied through delays D1 and D2 to the clear or reset input of flip-flop C. This changes flip-flop C to the ZERO state. Flip-flop D changes to the ZERO state by the change of flip-flop C from the ONE state to the ZERO state. The counter now contains 0000, and starts counting again with the next input pulse. The output of flip-flop D may be fed to another decade counter, which then counts by decimal 10's; its output can be fed to another that will count by 100's; and so on to the limit required of the equipment design.

g. Ring counter. This is another type of counter. In it the output of the last stage is connected to the input of the first stage. One of the stages is set to the ONE state; and the rest, in the ZERO state. The input pulse then moves the ONE state to succeeding stages with each input pulse.

There are many possible circuits for ring counters, just as there are for other type circuits. A 4-stage counter is shown in figure 7-7. In this circuit, if flip-flop A is in the ONE state and the other flip-flops are in the ZERO state, flip-flop A is the only one whose output is 1. The next input changes flip-flop A to the ZERO state but cannot affect the others since they are already in the ZERO state. However, the change of flip-flop A from the ONE state to the ZERO state causes flip-flop B to flip to the ONE state.

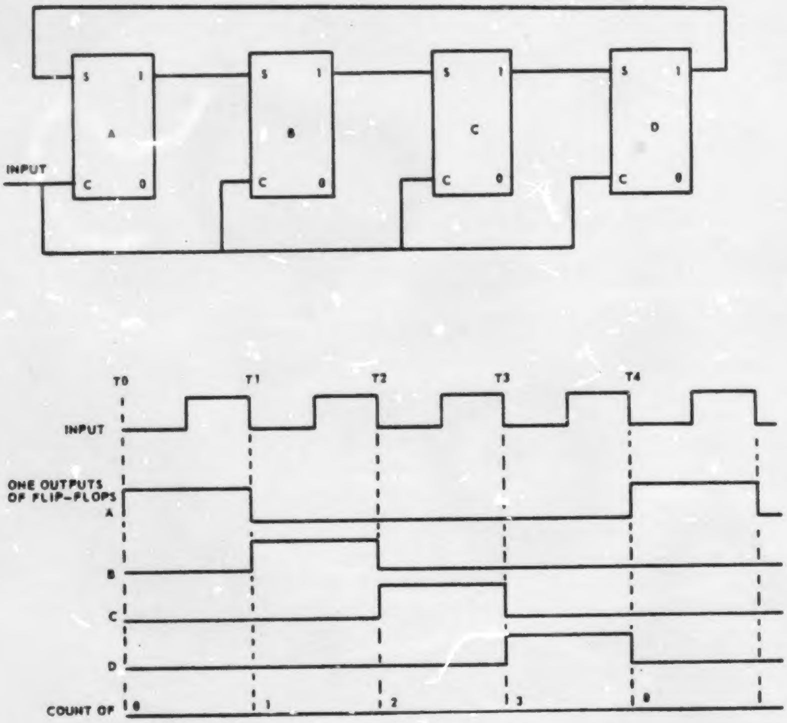


Fig 7-7. Ring counter.

In this manner, each input pulse changes the flip-flop that is in the ONE state to the ZERO state, and its change in state is used to set the next flip-flop to the ONE state. Thus, as the input pulses continue to come in, the conditions of the flip-flops will be:

D	C	B	A
0	0	0	1
0	0	1	0
0	1	0	0
1	0	0	0
0	0	0	1

(etc.)

You can see from the waveshapes shown in figure 7-7 that only one flip-flop is activated (in the ONE state) at any particular time. Also, there are only four possible states. Therefore, this 4 stage ring counter has a maximum number (called "modulus") of 4 discrete counts.

In computing machines, it is a common practice to assign one of the flip-flops the 0 count when it is in the ONE state, and to assign the following stages the 1, 2, 3, etc., counts, in sequence.

To illustrate, let us assign flip-flop A of figure 7-7 the 0 count when it is in the ONE state. In like manner, let flip-flop B represent the count of 1, flip-flop C the count of 2, and flip-flop D the count of 3. Assume that the counter is in the condition representing a 0 count. When the first pulse triggers the counter (at T_1), flip-flop A changes from the ONE state to the ZERO state, and the output from its ONE side changes flip-flop B to the ONE state. A count of 1 is now registered in the counter, because flip-flop B is in the ONE state. The count of 2 (T_2) is indicated by flip-flop C when it is set to the ONE state; and the count of 3, by flip-flop D in like manner at T_3.

A unique characteristic of ring counters is that only one output from a single flip-flop is required to indicate a given discrete count. In the equipment, each flip-flop output could "turn on" a single step or phase of a series of sequential operations. A ring counter of the type discussed could control up to 4 steps, since it has a modulus of 4. Because the modulus of the counter is determined by the number of stages, it is simply a matter of adding or subtracting stages to arrive at any desired modulus counter. For instance, a decade counter would have 10 stages, and could represent 0 through 9.

7-3. REGISTERS

A register is a group of storage devices or circuits for storing a unit of data. The most common unit of data is the word. Since information is usually moved about and operated upon in equipment word by word rather than bit by bit, a number of full-word registers is found in most digital equipment. The circuits must handle each individual bit, but the equipment can be so arranged that a group of circuits will usually handle a word at a time in response to an instruction or command.

Since the two principal methods of information transmission are parallel and serial, some registers are designed to take words in parallel form, and others take them in serial form. A third type is the series-parallel register which accepts the number or word bits in parallel form and feeds them out in serial form, or vice versa.

Registers have uses besides simple word storage. Frequently they are built for specific jobs such as counting or shifting. Counting has already been covered in the first part of this chapter; therefore our discussion here will be limited to storage and shift registers.

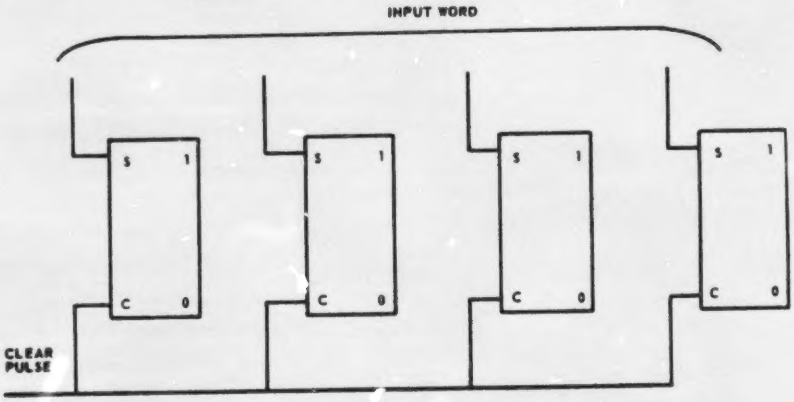


Fig 7-8. Parallel flip-flop register.

a. Storage register. The simplest registers are those used solely for word storage. Figure 7-8 shows one type of parallel flip-flop register that uses four flip-flops and can store a 4-bit word. The clear pulse clears all the flip-flops in the register to the ZERO state, erasing any information stored previously. The word to be stored is then applied in parallel form to the set inputs. The pulse in each bit position (where there is 1) sets the corresponding flip-flop in the register to the ONE state. No pulses appear in the bit positions where there are 0's, so the flip-flops in these positions remain in the ZERO state. The correct word is now stored in the register.

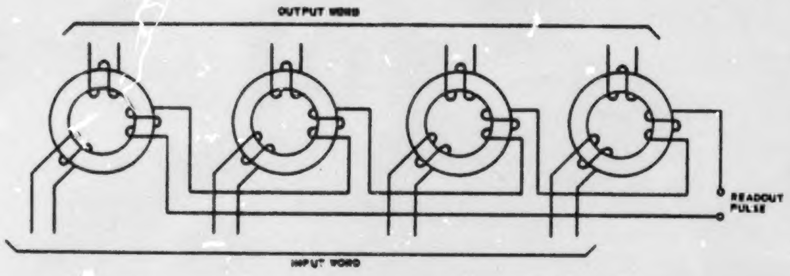


Fig 7-9. Parallel core register.

A parallel storage register of magnetic cores can be built similar to the one discussed. Figure 7-9 shows this type of register. Each bit of the input word is applied to the input winding of a separate core. The readout windings, connected either in series or in parallel, serve a dual purpose. When a readout pulse is applied, it not only reads out all the bits stored in the individual cores but also clears the register by resetting all cores to 0. The register is then ready to store a new word.

b. Shift register. A shift register is built with the intention of shifting any number stored in it for a purpose different from that of ordinary storage. It may be built to convert words from serial to parallel form or from parallel to serial form, or it may be used to multiply or divide the number by some power of 2. Remember that shifting a binary number one place to the left multiplies it by 2 and one place to the right divides it by 2.

One of the simplest shift registers is shown in figure 7-10. Only three stages are indicated, since the operation and connections would be the same for any number of stages. The register is arranged for a left shift. Each flip-flop is set to 1 or 0 when the word is written into the register. The outputs from the flip-flops are connected to AND gates 1, 2, 3, and 4, as shown.

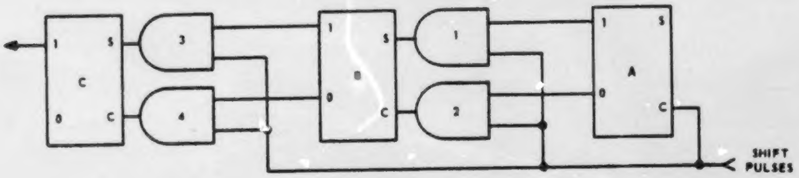


Fig 7-10. Shift register.

To see how the shift takes place, assume that 010 is stored in the register. Flip-flops C and A are in the ZERO state and flip-flop B is in the ONE state. From the flip-flops, gates 2 and 3 each have one activating level applied to them. Gates 1 and 4 each have nonactivating levels applied to them. When a shift pulse is applied, gates 2 and 3 are activated. Flip-flop A remains in the ZERO state, flip-flop B flips to the ZERO state, and flip-flop C sets to the ONE state. The register now contains 100. The original count of 010 has been shifted one place to the left.

To shift the information to the right, the gate and shift pulses could be connected so that the information moves from flip-flop C to flip-flop B to flip-flop A. In some applications it is desirable to be able to shift in either direction. A register can be made to do this by using two sets of gates and transfer lines with each set having its own shift pulse line. A pulse on one line would provide a shift to the right, and a pulse on the other would provide a shift to the left.

The logic diagrams for shift registers are shown in figure 7-11.

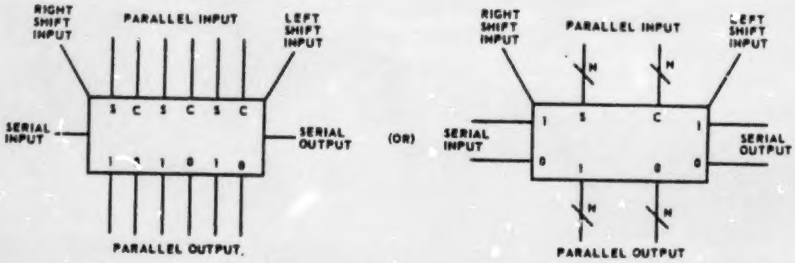

RIGHT SHIFT INPUT
PARALLEL INPUT
LEFT SHIFT INPUT
SERIAL INPUT
S C S C S C
1 0 1 0 1 0
SERIAL OUTPUT
PARALLEL OUTPUT
(OR)
RIGHT SHIFT INPUT
PARALLEL INPUT
LEFT SHIFT INPUT
N
N
SERIAL INPUT
1
0
S
C
1
0
1
0
SERIAL OUTPUT
N
N
PARALLEL OUTPUT

Fig 7-11. Logic symbols for shift registers.

Another type of shift register employs the metallic-ribbon storage device (discussed in chapter 6). The magnetic-shift register uses the single-diode transfer loop to transfer the information from one core to the next. (How this is done was also covered in chapter 6.)

Figure 7-12 shows a 4-core magnetic shift register that stores two bits of information. The information is applied to L0. The shift pulses are applied to transfer windings L1, L4, L7, and L10. To carry the register through a cycle of shift-in and shift-out, let us assume that prior to shift-in, cores A through D are in the ZERO state.

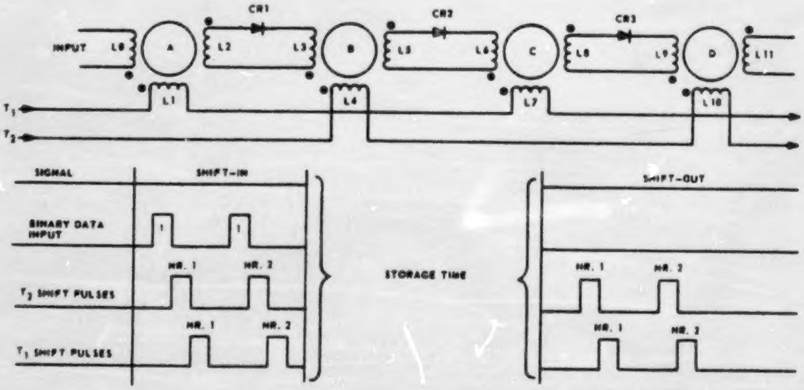

CR1
CR2
CR3
INPUT
L0
A
L2
L3
B
L5
L6
C
L8
L9
D
L11
L1
L4
L7
L10
T_1
T_2
SIGNAL
SHIFT-IN
BINARY DATA INPUT
1
1
NR. 1
NR. 2
T_2 SHIFT PULSES
NR. 1
NR. 2
T_1 SHIFT PULSES
STORAGE TIME
SHIFT-OUT
NR. 1
NR. 2
NR. 1
NR. 2

Fig 7-12. Magnetic shift register.

The first data pulse, which represents a binary 1, is applied to L0 of core A. Core A switches to the ONE state. The data in each core of the register is now:

Core	A	B	C	D
Data	1	0	0	0

The next pulse, which is applied to line T2, is shift pulse number 1. It is applied to L4 and L10 on the T2 line. If a binary 1 were in core B or core D, it would be transferred to core C or out, respectively.

The data in the register is still:

Core	A	B	C	D
Data	1	0	0	0

The next pulse is shift pulse number 1 on the T1 line. It is applied to L1 and L7. The 1 in core A is shifted to core B, and 0 is in core C, so no shift takes place from C to D. The data in the register is now:

Core	A	B	C	D
Data	0	1	0	0

The next pulse is the second data pulse. It is applied to L0 and switches core A to the ONE state. The data in the register is now:

Core	A	B	C	D
Data	1	1	0	0

The next pulse is the shift pulse number 2 on the T2 line. It is again applied to L4 and L10. The binary 1 in core B is shifted to core C. There is a binary 0 in core D, so no shift-out takes place. The data in the register is now:

Core	A	B	C	D
Data	1	0	1	0

The last pulse in the shift-in process is pulse number 2 on the T1 line. This is applied to L1 and L7. The binary 1's in cores A and C are shifted to cores B and D. The data in the register is now:

Core	A	B	C	D
Data	0	1	0	1

This completes the shift-in. The data is now stored in the cores and could remain in storage indefinitely.

The shift-out is initiated by T2 shift-out pulse number 1. It is applied to L4 and L10. The 1 in core B will be shifted to core C and the 1 in core D is shifted out. The data in the register is now:

Core	A	B	C	D
Data	0	0	1	0

The next pulse is T1 shift-out pulse number 1. It is applied to L1 and L7. The data in core A is a 0, so no shift takes place. The 1 in core C is transferred to core D. The data in the register is now:

Core	A	B	C	D
Data	0	0	0	1

The next pulse applied is T2 shift-out pulse number 2. It is applied to L4 and L10. There is a 0 in core B, so no shift takes place. The 1 in core D is shifted out. The data in the register is now:

Core	A	B	C	D
Data	0	0	0	0

The last pulse applied is the T1 shift-out pulse number 2. It has no effect on the cores B and D, since they are in the ZERO state. The shift-out is now complete.

7-4. ADDERS

The purpose of the adder circuit is to sum binary numbers in accordance with the rules for binary addition:

A + B = SUM
0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 0 with a carry of 1

Observe that the sum is 1 only when A and B are dissimilar; that is, when A is 1 and B is 0, or when A is 0 and B is 1. If A and B are both 0, the sum is 0. If A and B are both 1, the sum is the binary number 10; this is expressed as a sum of 0 with a carry of 1 to the next higher order column. Hence, the sum function coincides with the EXCLUSIVE OR function (sometimes called a quarter-adder because it accomplishes approximately one-fourth of the addition process). The carry function coincides with the AND function. The Boolean expressions are:

$$A\bar{B} + \bar{A}B = S \text{ (sum)}$$
$$AB = C \text{ (carry)}$$

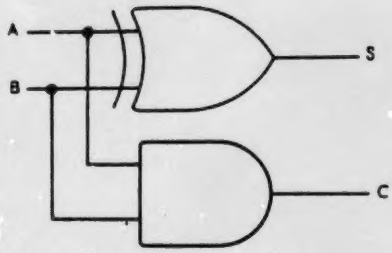
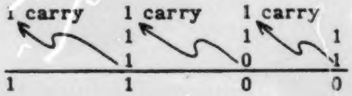
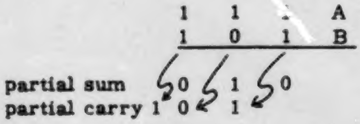


Fig 7-13. Half-adder circuit.

a. Half-adder. The circuit for these expressions (fig 7-13) is referred to as a half-adder. It can add only the least significant place column, since it has no provision for adding the carry from a lower order place column. For example, assume that the binary number 111 is to be added to the binary number 101. The binary addition is performed as follows:



A half-adder at each place position will generate a partial sum and a partial carry:



The half-adder in the LSD position, having no previous carry to consider, generates a sum of ZERO and a ONE carry to the next higher place position. This second position half-adder generates a sum of ONE with a ZERO carry. But it cannot consider the previous carry from the LSD position.

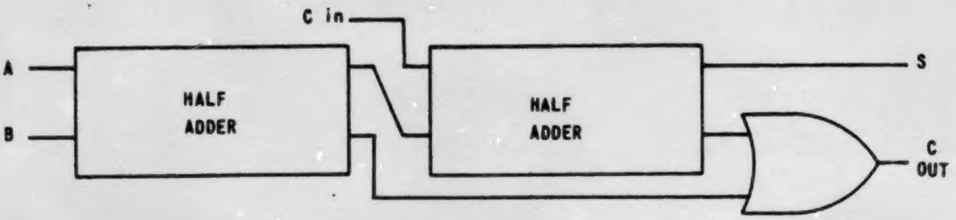
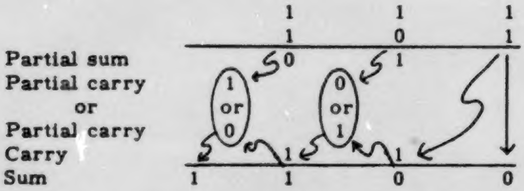

C in
A
B
HALF ADDER
HALF ADDER
S
C OUT

Fig 7-14. Full adder.

b. Full-adder. Two half-adders and an OR gate comprise a full-adder (fig 7-14). A full-adder, by considering a previous carry, can accomplish addition in the higher place positions:


1 1 1
1 0 1
Partial sum
Partial carry
or
Partial carry
Carry
Sum
0
1
1 or 0
0 or 1
1
1
1 1 0 0

A half-adder in the LSD position generates a sum of ZERO and a carry of ONE to the next higher place position. The first half-adder in the second place position generates a partial sum of ONE and a partial carry of ZERO. The partial sum and the carry from the LSD position are added by the second half-adder generating a sum of ZERO and a partial carry of ONE. The partial carry from the two half-adders are OR'ed to generate a carry of ONE to the next higher place position. The first half-adder in the third place position generates a partial sum of ZERO and a partial carry of ONE. The second half-adder generates a sum of ONE and a partial carry of ZERO. The OR gate generates a carry of ONE to the next higher place position.

(1) A parallel adder requires a full-adder for each place position, except the LSD which needs a half-adder only (fig 7-15). Each carry output is applied to the carry input of the next higher place position.

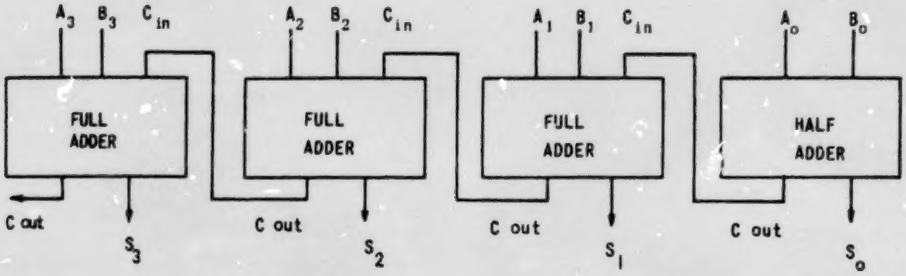

A_3 B_3 C_{in}
A_2 B_2 C_{in}
A_1 B_1 C_{in}
A_0 B_0
FULL ADDER
FULL ADDER
FULL ADDER
HALF ADDER
C out
C out
C out
C out
S_3
S_2
S_1
S_0

Fig 7-15. Parallel adder.

(2) A serial adder requires one full-adder and a delay line with a delay equal to the period of one shift pulse (fig 7-16). The binary numbers to be added arrive at the adder LSD first. The carry output for each place position is delayed until the time the next higher place position is arriving at the adder.

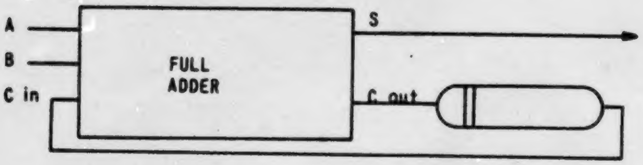


Fig 7-16. Serial adder.

7-5. DECODERS

A decoder is a combination of switching circuits used to translate two or more input signals in code form into a single discrete output signal. A decoder can perform a number of functions; i. e., it may be used to detect one of many counts in a counter or register. Since the operation of digital equipment is based on logical timing, the output of a decoder may be used to end an operation or to start an operation. For instance, if a certain operation has 3 steps, a decoder connected to a counter detects the count of 3, produces an output at that time, and stops the operation or causes the equipment to proceed to the next operation.

A decoder for detecting the count of 3 is shown in figure 7-17. Flip-flops A, B, and C make a binary up-counter. Gate 1 is an AND gate with inputs from the ONE sides of flip-flops A and B and the ZERO side of flip-flop C. --Why are the connections made in this way?--Binary 3 is 011. This means that with a count of 3 in the counter, flip-flops A and B are in the ONE state and flip-flop C is in the ZERO state. At this time, gate 1 has all its activating signals present, so it will have an output pulse. With any other count in the counter, the gate would not be activated.

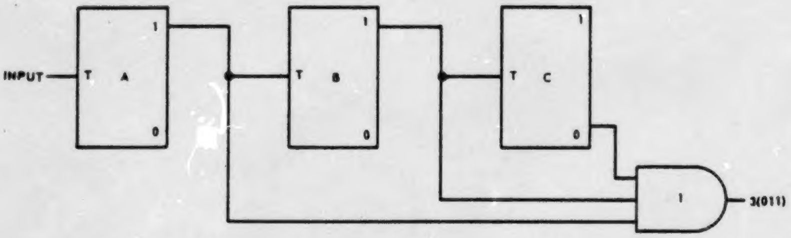


Fig 7-17. Decoder for count detection.

It is easy to determine the number that a decoder will detect. Starting with the most significant flip-flop (C in fig 7-17), write 1 if the gate is connected to the ONE side and a 0 if the gate is connected to the ZERO side. The result is the number detected in binary form. The example in figure 7-17 is 011, which is 3.

To determine the proper connections that must be made to detect a certain number, write the desired number in binary form. A binary 1 represents a ONE-side connection, and a binary 0 represents a ZERO-side connection. For example, to detect a count of 5 from the computer in figure 7-17, write 5 in binary notation. This is 101. The AND gate must have connections to the ONE side of flip-flops A and C and to the ZERO side of flip-flop B. Note that the least significant digit in the binary number represents the connection from the gate to the least significant flip-flop, which is the input flip-flop of the counter.

It is also possible to detect the NOT function of a number. That is, the decoder detects all the numbers in the counter except one certain number. Figure 7-18 shows a decoder that detects the NOT function of 3. Notice that the gate is an OR circuit and that the connections to the flip-flops are opposite to the connections in figure 7-17. This is consistent with the rules of Boolean algebra. The equation for the output of gate 1 in figure 7-17 is $3 = AB\bar{C}$. Applying DeMorgan's theorem, $3 = \bar{A} + \bar{B} + C$. In these equations, A, B, and C are the ONE-side outputs of the flip-flops; and $\bar{A}$, $\bar{B}$, and $\bar{C}$ are the ZERO-side outputs of the flip-flops.

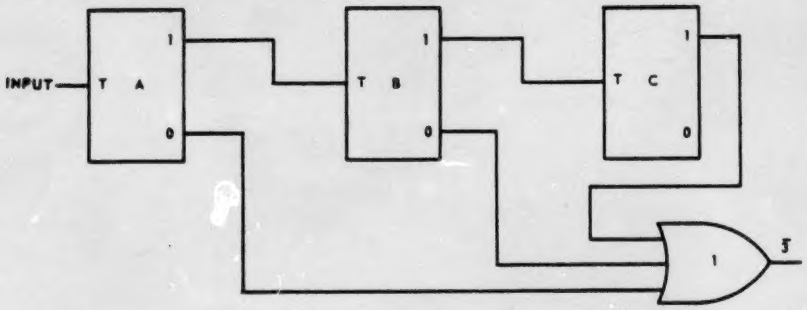


Fig 7-18. Decoder for NOT function detection.

a. Matrices. The decoder arrangements considered above are the types that produce a single output, usually from two or more inputs. Another type is the multiple-output switching network, called a matrix. It produces a different output for each different input or combination of inputs. The matrix gets its name from the manner in which it is drawn schematically (and often built) with components and connections arranged in rows and columns.

One type of matrix is made of diodes. Figure 7-19 shows a diode matrix that is used to detect the count of 0 through 9. The matrix is composed of 10 diode AND gates, each having four inputs. Each gate detects only one number. The Boolean equations for counts 0 through 9 are as follows:

Decimal Number	Binary Number	Equation
0	0000	$\overline{D}\,\overline{C}\,\overline{B}\,\overline{A}$
1	0001	$\overline{D}\,\overline{C}\,\overline{B}\,A$
2	0010	$\overline{D}\,\overline{C}\,B\,\overline{A}$
3	0011	$\overline{D}\,\overline{C}\,B\,A$
4	0100	$\overline{D}\,C\,\overline{B}\,\overline{A}$
5	0101	$\overline{D}\,C\,\overline{B}\,A$
6	0110	$\overline{D}\,C\,B\,\overline{A}$
7	0111	$\overline{D}\,C\,B\,A$
8	1000	$D\,\overline{C}\,\overline{B}\,\overline{A}$
9	1001	$D\,\overline{C}\,\overline{B}\,A$

The network detects a number in the same manner as explained for the network in figure 7-17. Let's assume that the counter has a count of 0000 in it. In this case, all of the flip-flops are in the ZERO state. From figure 7-19 you can see that for the 0 line, inputs to the diode gate are from the ZERO sides of all the counter flip-flops. With all flip-flops in the ZERO state, the gate is activated and an activated signal is felt on line 0. Assume that the counter is stepped to a count of 0001. Notice that the 1 line has gate inputs from the ONE side of flip-flop A and from the ZERO sides of flip-flops B, C, and D. With 0001 in the counter, all the activating signals for the 1 line gate are present. Therefore, the 1 line now has an activated signal on it. As the counter counts, each count is detected in the same manner.

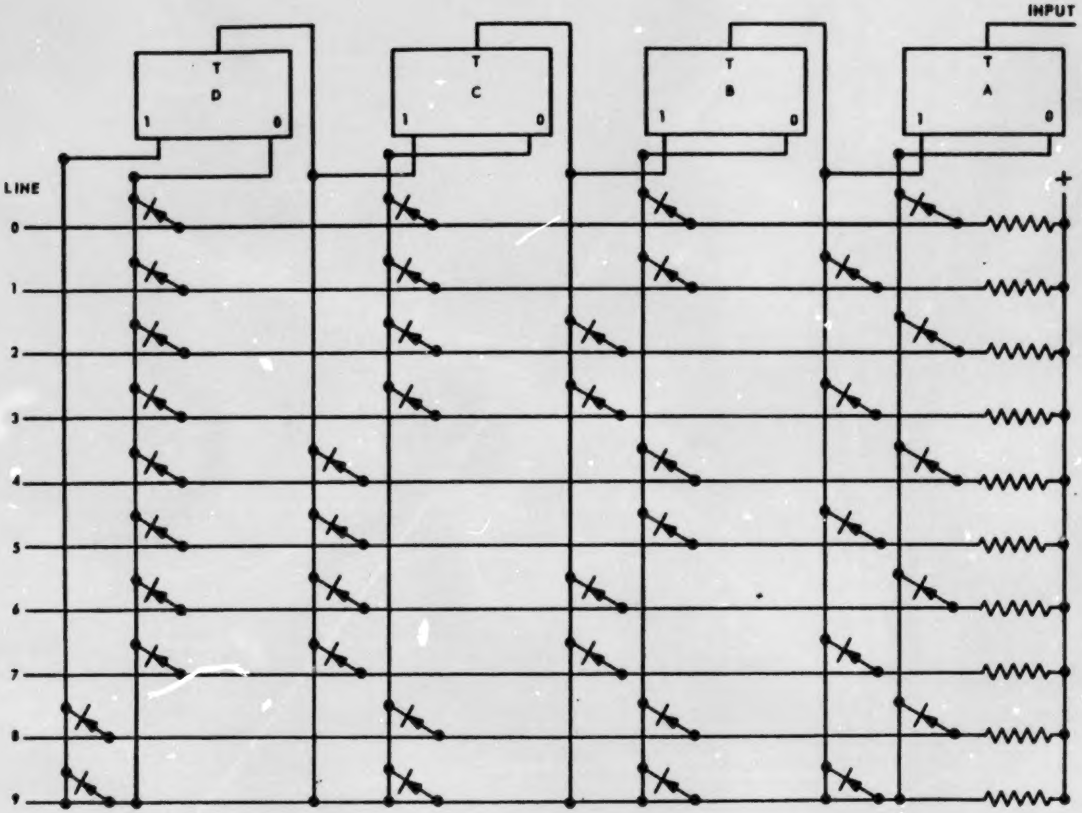

INPUT
T
D
1
0
T
C
1
0
T
B
1
0
T
A
1
0
LINE
+
0
1
2
3
4
5
6
7
8
9

Fig 7-19. Diode matrix.

Another type of matrix is the transistor matrix. It is composed of vertical and horizontal lines with a transistor at each intersecting line. When a vertical and a horizontal line are selected, the transistor at the point of intersection is turned on to give an output. A transistor matrix will accept two coordinate input signals and produce a single output signal.

Figure 7-20 shows a 4 X 4 transistor matrix. Transistors Q1, Q6, Q11, and Q16 are the horizontal inputs; and transistors Q21, Q22, Q23, and Q24 are the vertical inputs. The collector of each horizontal input transistor is tied to the base of four transistors. When a horizontal input transistor is turned off, it will apply a negative potential to the base of the four transistors in a horizontal line. The collector of each vertical input transistor is tied to the emitter of four transistors. When a vertical transistor is turned on, it provides a current path for four transistors in a vertical line.

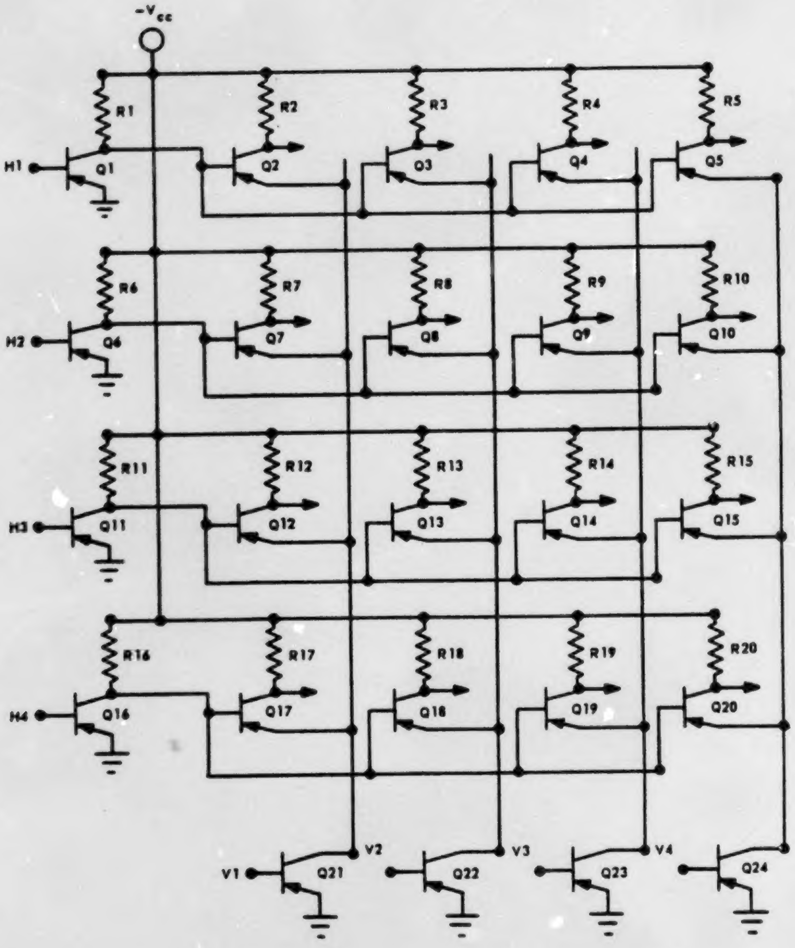

$-V_{cc}$
R1
R2
R3
R4
R5
H1
Q1
Q2
Q3
Q4
Q5
R6
R7
R8
R9
R10
H2
Q6
Q7
Q8
Q9
Q10
R11
R12
R13
R14
R15
H3
Q11
Q12
Q13
Q14
Q15
R16
R17
R18
R19
R20
H4
Q16
Q17
Q18
Q19
Q20
V2
V3
V4
V1
Q21
Q22
Q23
Q24

Fig 7-20. Transistor matrix.

Referring to figure 7-20, let us see how one output can be obtained by applying two inputs. Assume that prior to the application of horizontal input signal, Q1, Q6, Q11, and Q16 are conducting. This places approximately 0 volts on the bases of all transistors at the intersections. Assume also that Q21, Q22, Q23, and Q24 are at cutoff. This leaves the emitters of the transistors with no emitter current path. A positive input signal to horizontal line H2 cuts off Q6. This places $-V_{cc}$ on the bases of transistors Q7, Q8, Q9, and Q10. These transistors try to conduct, but their emitters are tied to the vertical input transistors. A negative input signal to vertical line V2 causes Q22 to conduct through Q8. The collector voltage of Q8 goes toward ground potential from $-V_{cc}$. Q7, Q9, and Q10 cannot conduct since Q21, Q23, and Q24 are still cut off. Thus, for these two input signals, one output signal is obtained. Any one of the 16 transistors at the intersections may be activated in the same manner. This technique is referred to as addressing the activated transistor or its output line.

b. Digital-to-analog decoder. An output consisting of digital data may be sent to a digital-to-analog converter to change it from a digital form to an analog voltage. This voltage may be used to control some mechanisms; for instance, it can drive an antenna or position the electron beam in a CRT.

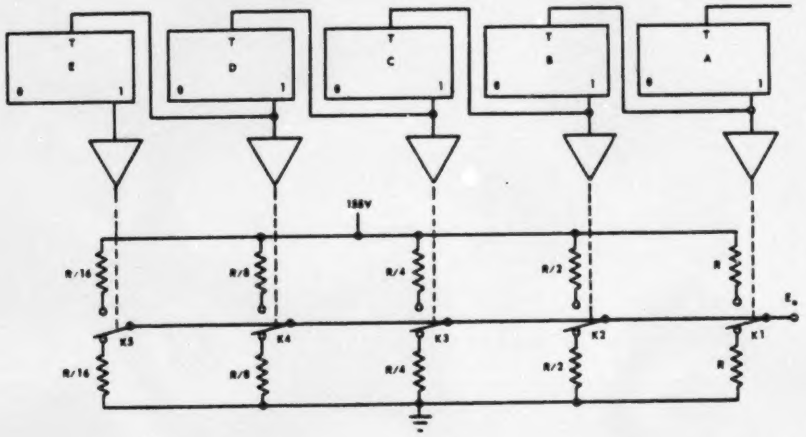


Fig 7-21. Digital-to-analog converter.

Of the several ways of converting digital data to analog, one of the most common is by use of a resistor network. In the typical digital-to-analog circuit shown in figure 7-21, the converter is connected to a 5-stage counter that holds a maximum decimal count of 31. The resistor network is made up of two sections which contain identical pairs of resistors in each leg. Notice that the value of each resistor is halved as the number increases from the LSD to the MSD. The output from the ONE side of each flip-flop is applied to a relay driver, such as the one discussed in chapter 5. When any one of the flip-flops is in the ONE state, the corresponding relay is energized. For instance, if flip-flop D is in the ONE state, relay K4 will be energized. With this arrangement, the count in the counter is converted from its digital form to a voltage proportional to that count. For example, if an output of 5 volts equals a count of 1, then an output of 10 volts equals a count of 2.

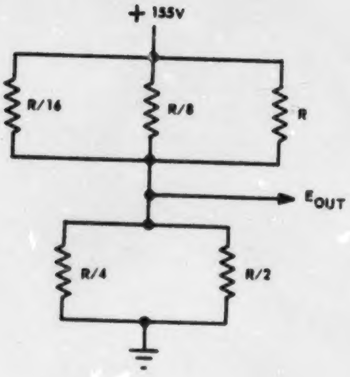


Fig 7-22. Equivalent circuit with count of 11001.

With a count of 11001 or decimal 25 in the counter in figure 7-21, relays K5, K4, and K1 are energized. This gives an equivalent network, as shown in figure 7-22.

The total resistance, R_o, of the upper ladder is:

$$\frac{1}{R_o} = \frac{1}{R/16} + \frac{1}{R/8} + \frac{1}{R}$$

$$\frac{1}{R_o} = \frac{16}{R} + \frac{8}{R} + \frac{1}{R}$$

$$\frac{1}{R_o} = \frac{25}{R}$$

$$R_o = \frac{R}{25}$$

The total resistance, R_f, of the lower ladder is:

$$\frac{1}{R_f} = \frac{1}{R/4} + \frac{1}{R/2}$$

$$\frac{1}{R_f} = \frac{4}{R} + \frac{2}{R}$$

$$\frac{1}{R_f} = \frac{6}{R}$$

$$R_f = \frac{R}{6}$$

The total resistance, R_t, of the entire resistor network is:

$$R_t = \frac{R}{25} + \frac{R}{6}$$

$$R_t = \frac{6R + 25R}{150}$$

$$R_t = \frac{31R}{150}$$

The voltage E_{out} is:

$$E_{out} = \frac{R_f}{R_t} \times 155v$$

$$E_{out} = \frac{\frac{R}{6}}{\frac{31R}{150}} \times 155$$

$$E_{out} = \frac{R}{6} \times \frac{150}{31R} \times 155$$

$$E_{out} = 125 \text{ volts}$$

Note the ratio between R_f and R_t:

$$\frac{R_f}{R_t} = \frac{\frac{R}{6}}{\frac{31R}{150}}$$

$$\frac{R_f}{R_t} = \frac{R}{6} \times \frac{150}{31R}$$

$$\frac{R_f}{R_t} = \frac{25}{31}$$

The count in the counter is 25, and the maximum count of the counter is 31. So, instead of solving for the output by the method that we used before, the output may be found by the formula:

$$E_{out} = E_a \times \frac{R_f}{R_t}$$

where

E_a = applied voltage
R_f = count in the counter
R_t = maximum count of counter

The problem just solved would be:

$$E_{out} = 155 \times \frac{25}{31}$$

$$E_{out} = 125 \text{ volts}$$

7-6. ANALOG-TO-DIGITAL ENCODER

Not all inputs to digital equipment are in digital form. Some are in the form of analog voltages that represent quantities. Some analog quantities that are applied directly represent speed of movement, speed of rotation, position of a shaft, elevation, temperature, pressure, and humidity. Before this information can be used by digital equipment, it must be converted to digital form. An analog-to-digital converter does this job.

a. Shaft position encoder. A type of converter that converts a shaft position to a digital number is shown in figure 7-23. There are many different types of converters used for this purpose. The one explained is typical. The conducting material in the disk (fig 7-23) is shown in the dark areas, and the nonconducting material is shown in the light areas. Contacts are arranged into as many channels as there are digits in the largest binary number to be coded. A brush is in contact with each channel on the disk. A voltage source is used in the circuit so that if the brush is in contact with the conducting material, a binary 1 is detected. If the brush is in contact with the insulating material, a binary 0 is detected. The binary number detected in the position shown in figure 7-23 is 0000. As the shaft rotates counterclockwise, the brush in the outer channel makes contact with the shaded area. The count detected is binary 0001. As the converter continues to rotate, the binary count detected increases, as shown around the circumferences of the converter in figure 7-23. This digital information may now be fed into the equipment.

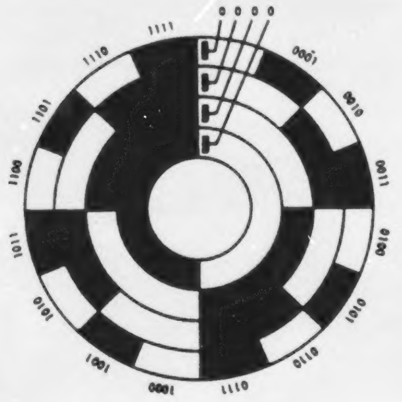


Fig 7-23. Binary shaft position encoder.

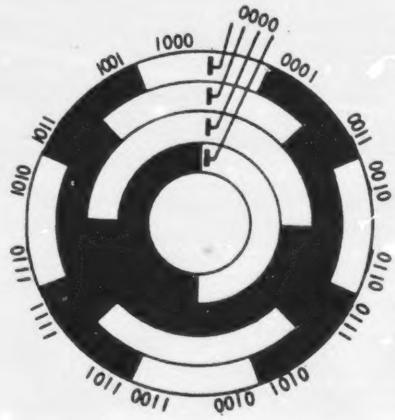


Fig 7-24. Shaft position encoder using Gray code.

(1) When more than one channel changes states between consecutive counts, errors may be produced. For example, in going from a count of 0111 to 1000, the MSD brush will make contact before the three lower order brushes break contact. Thus, an erroneous 1111 count is produced due to the brushes having a finite width. Imperfections in brush alignment also produce errors.

(2) The Gray code, in which only one digit or channel changes states between consecutive counts, was developed to eliminate this problem. A shaft-position encoder using the Gray code is shown in figure 7-24. The Gray code does not lend itself to arithmetic operations, and must be converted to pure binary as explained in chapter 2.

b. Ramp voltage encoder. A type of converter used to convert an analog voltage into a digital number is shown in the block diagram of figure 7-25. Typically, a digital counter is started when a sawtooth ramp voltage crosses the zero reference, and it is stopped when it equals the applied analog voltage. The count remaining in the counter is the digital value of the analog voltage.

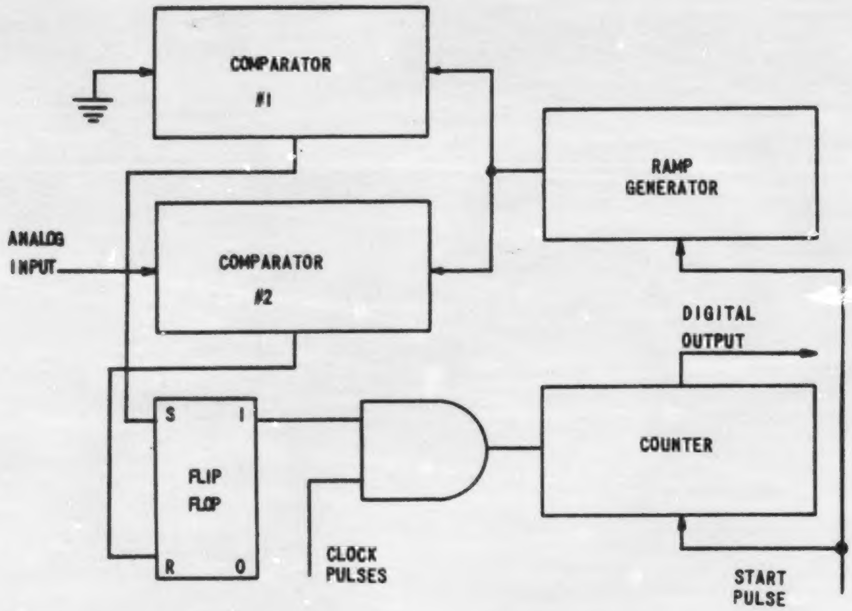


Fig 7-25. Ramp voltage encoder.

(1) A start pulse resets the counter to zero and restarts the ramp generator at some negative voltage. The rising ramp voltage reaches the linear portion of its waveform before crossing the zero reference. The output of the ramp generator is fed to two comparators.

(2) Each comparator has two inputs and acts to produce an output when the voltage of one input exceeds that of the other. The second input to comparator #1 is ground or the zero reference while that of #2 is the analog input.

(3) Comparator #1 compares the rising ramp voltage to the zero reference and produces an output when the ramp exceeds zero. This output sets the flip-flop to the ONE state, which enables the AND gate and allows the counter to start counting clock pulses.

(4) Comparator #2 compares the rising ramp voltage with the analog input and produces an output when the ramp voltage becomes greater than the analog voltage. This output resets the flip-flop, which disables the AND gate and stops the counter.

(5) The clock pulses are timed to the slope of the ramp so that the count in the counter is the digital value of the analog input voltage. The digital output is then taken from the counter before the next start pulse.

7-7. SUMMARY

a. Logic circuits perform the basic functions of counting, storing, comparing, and transferring information. Counters are made of flip-flops connected in series or parallel. A counter may count up or count down, depending on whether the connections are made from the ONE or the ZERO sides of the flip-flops. The maximum number that a flip-flop counter will hold is determined by the number of flip-flops used. The parallel counter is faster than the serial counter but requires more circuitry. The serial counter has its input pulse applied to the flip-flop that represents the LSD of the count. Each flip-flop is flipped by the change of state of the preceding flip-flop. The inputs to a parallel counter are applied through gates to the input of each of the flip-flops in the counter.

b. Counters may be connected as binary, decade, or ring counters. The states of a binary counter represent the binary form of a number; it will count to the maximum count of the counter, reset to zero, and start the count over. The states of a decade counter represent the 10 digits of the decimal system; it will count to 9, reset to zero, and start the count over. A ring counter has only one flip-flop in the ONE state at any given time. The ONE state moves from one flip-flop to the next after each input pulse. The output is fed back to the input, and the counter starts the count over.

c. A register is used to store information or to shift data. Storage registers may be serial, parallel, or a combination. Shift registers are used to shift data right or left. Registers may be made from flip-flops or magnetic cores.

d. Adders are used to sum binary numbers. Half-adders can be used to add the LSD column, but two half-adders (a full-adder) must be used when a carry from a lower order column is to be added.

e. A decoder is used to detect when a counter or register contains a specified count. It may also be used to convert a binary configuration to an analog voltage.

f. An analog-to-digital encoder is used to convert an analog input to a binary configuration. Such inputs may be mechanical, as in the shaft position encoder; or electrical, as in the ramp voltage encoder.

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117

FUNDAMENTALS OF DIGITAL LOGIC

Course Introduction

FUNDAMENTALS OF DIGITAL LOGIC is designed to prepare electronics personnel for further training in digital techniques. It presents need-to-know information that is basic to any maintenance course on digital equipment.--As this instruction includes digital circuits using semiconductors, students must have previous knowledge of transistors.

ORDER OF STUDIES

Lesson Number	Study Hours	Reserve Retirement Credits	Subject Matter
1	3	1	Binary Arithmetic
2	3	1	Boolean Algebra
3	2	0	Logic Gates
4	2	1	Logic Flip-Flops; Nonlogic Circuits; Magnetic Cores
5	2	1	Logic Circuits
	2	1	FINAL EXAMINATION
	14	5	

EXAMINATION: Supervised final examination without textbook or notes; time limit, 2 hours.

MATERIALS: MCI 28.6d, Fundamentals of Digital Logic.

Lesson sheets and answer sheets.

RETURN OF MATERIALS: Students who successfully complete this course are permitted to keep the course materials.

Students disenrolled for inactivity or at the request of their commanding officer will return all course materials.

PREREQUISITE: An assigned MOS in OF 28, 59, or 62; or completion of any course in MCI's 28, 62, or 66 series.

7-1

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FUNDAMENTALS OF DIGITAL LOGIC

Lesson 1

Binary Arithmetic

STUDY ASSIGNMENT: Information for MCI Students.
Course Introduction.
MCI 28.6d, Fundamentals of Digital Logic, chap 1.

WRITTEN ASSIGNMENT:

A. Multiple Choice: Select the ONE answer which BEST completes the statement or answers the question. After the corresponding number on the answer sheet, blacken the appropriate box.

Value: 1 point each

1. What number system is most commonly used in digital equipment?

    a. Binary
    b. Ternary
    c. Octal
    d. Decimal

2. Divide 110110_2 by 1001_2.

    a. 101
    b. 110
    c. 111
    d. 1110

3. Divide 11001_2 by 101_2.

    a. 11
    b. 100
    c. 101
    d. 1001

4. Divide 1000010_2 by 1011_2.

    a. 110
    b. 111
    c. 1000
    d. 1011

5. Subtract 11_2 from 1101001_2.

    a. 101101
    b. 1011110
    c. 1100110
    d. 1101000

6. Subtract 111010_2 from 11101111_2.

    a. 10010101
    b. 10110101
    c. 10111101
    d. 1100101

7. Subtract 11_2 from 101_2.

   a. 1
   b. 10
   c. 11
   d. 100

8. Add 1011_2 and 1_2.

   a. 1010
   b. 1100
   c. 1101
   d. 1111

9. Subtract 110011_2 from 1101101_2.

   a. 101110
   b. 110110
   c. 111000
   d. 111010

10. Convert 7775_{10} to an octal.

    a. 14237
    b. 15137
    c. 17135
    d. 17137

11. Add 101111111_2 and 11_2.

    a. 101111000
    b. 101111010
    c. 110000010
    d. 110000110

12. Convert 1111111_2 to a decimal.

    a. 63
    b. 64
    c. 127
    d. 255

13. Add 11111_2, 1111_2, 111_2, and 11_2.

    a. 111000
    b. 111100
    c. 1011000
    d. 1011010

14. Add 11011_2, 111_2, 101_2 and 11_2.

    a. 100110
    b. 101010
    c. 101011
    d. 110110

15. The decimal number system was invented by the

    a. Romans.
    b. Hindus.
    c. Arabs.
    d. Germans.

16. The point used in a base 8 number system is a(an) _____ point.

    a. binary
    b. octal
    c. decimal
    d. fractional

17. The number of different symbols and digits used in a number system is called the

    a. level.
    b. subscript.
    c. status indicator.
    d. radix.

18. Multiply 111111_2 by 1001_2.

    a. 10111101
    b. 111000111
    c. 1000110111
    d. 1100110111

120

19. The code developed to reduce the degree of error which might occur when numbers are transferred is called the

a. binary coded decimal.
b. biquinary code.
c. end-around-carry.
d. Gray code.

20. The binary equivalent for 1263.4_8 is

a. 1010110.100
b. 1010110011.1
c. 110110011.100
d. 100010110011.1

21. 110101100_2 converted to an octal is

a. 408.
b. 426.
c. 574.
d. 654.

22. 1001 in the binary coded decimal system converted to a decimal number is

a. 9.
b. 11.
c. 13.
d. 15.

23. The binary equivalent for 706_8 is

a. 111101.
b. 1110101.
c. 1110110.
d. 111000110.

24. Convert 7431_8 to a binary.

a. 111100011001
b. 111100101011
c. 110110111
d. 1111011111

25. The octal equivalent for 9_{10} is

a. 6.
b. 7.
c. 11.
d. 13.

26. 48_{10} converted to a binary is

a. 11000.
b. 10100.
c. 110010.
d. 110000.

27. Multiply 11011_2 by 11_2.

a. 111011
b. 1001011
c. 1010001
d. 1101101

28. Multiply 1101_2 by 10_2.

a. 11010
b. 11011
c. 11110
d. 110110

29. Convert 7775_8 to a decimal.

a. 2045
b. 2047
c. 4093
d. 4095

30. 110011_2 converted to a decimal is

a. 27.
b. 35.
c. 51.
d. 99.

31. 11011011_2 converted to an octal is

a. 333.
b. 453.
c. 633.
d. 663.

32. 144_{10} converted to an octal is

a. 100.
b. 200.
c. 220.
d. 2020.

33. 621_8 converted to a decimal is

a. 401.
b. 408.
c. 468.
d. 501.

34. The zero is always used as a

a. place holder.
b. carry.
c. positive quantity.
d. count of 10.

35. How many Arabic numerals are there?

a. 9
b. 10
c. 12
d. 16

36. The three digits used in the ternary number system are

a. 3, 4, 5.
b. 2, 3, 0.
c. 1, 2, 3.
d. 0, 1, 2.

Total Points: 36

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FUNDAMENTALS OF DIGITAL LOGIC

Lesson 2

Boolean Algebra

STUDY ASSIGNMENT: MCI 28.6d, Fundamentals of Digital Logic, chap 2.

WRITTEN ASSIGNMENT:

A. Multiple Choice. Select the ONE answer which BEST completes the statement or answers the question. After the corresponding number on the answer sheet, bl en the appropriate box.

Value: 1 point each

1. The sign (+) in a Boolean expression indicates _____ addition.

a. arithmetic
b. algebraic
c. logical
d. binary

2. The expression $(\overline{A} \cdot \overline{B})$ is equivalent to

a. $(\underline{\overline{A}} + \underline{\overline{B}})$
b. $(A \cdot B)$
c. $(\overline{A + B})$
d. $(A + B)$

3. The NOT sign over an expression is used to denote the signal's

a. presence.
b. complement.
c. level.
d. function.

4. Boolean algebra is used to represent the _____ of electrical circuits.

a. theory
b. maintenance
c. miniaturization
d. function

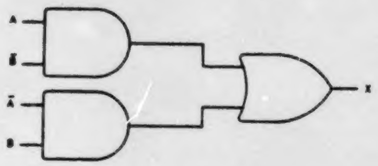
5. Which number system is used with Boolean algebra?

a. Binary
b. Ternary
c. Octal
d. Decimal

6. Which is NOT a Boolean expression?

a. $A + B$
b. $A - B$
c. $\underline{A} \cdot \underline{B}$
d. $\overline{A} \cdot B$

7. Which is the Boolean equation for this diagram?



a. $X = (AB) + (AB)$
b. $X = \underline{A}B$
c. $X = \underline{A}B$
d. $X = (\overline{A}B) + (A\overline{B})$

8. The diagram in question 7 would most likely represent

   a. an ordinary switching circuit in an ignition system.
   b. the circuit for an inclusive OR gate.
   c. the circuit for an exclusive AND gate.
   d. a switching circuit used to turn something on or off from two different sources.

9. The result of double complementation of a signal is

   a. logical inversion.
   b. logical addition.
   c. logical multiplication.
   d. no change.

10. The basic application of Boolean algebra is to

    a. design digital circuits.
    b. express logic functions mathematically.
    c. use binary numbers.
    d. extend the uses of ordinary algebra.

11. Which is equivalent to the Boolean expression A+B?

    a. A NOT B
    b. A OR B
    c. A PLUS B
    d. A AND B

12. Expressions that indicate logical multiplication involving only one variable are called _____ theorems.

    a. absorption
    b. common-identity
    c. distributive
    d. intersection

13. You begin writing an equation for a logic diagram by writing the output for

    a. the total diagram.
    b. one branch from the output gate.
    c. the input gate(s).
    d. either the output or input gate(s).

14. In the Boolean equation A + B = X, there are _____ possible numerical combinations.

    a. 2
    b. 3
    c. 4
    d. 8

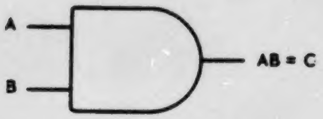
15. A gate will be inhibited when the input signals

    a. do not agree with the state indicators.
    b. are all HIGHS.
    c. are all LOWS.
    d. are both HIGHS and LOWS.

16. Which is the basic reason for applying Boolean algebra theorems to Boolean algebra equations?

    a. Rearrangement
    b. Simplification
    c. Complementation
    d. Logical addition

17. The Boolean function represented by the circuit shown in this figure is the _____ function.



    a. EXCLUSIVE OR
    b. INCLUSIVE OR
    c. NOT
    d. AND

18. What type of switch circuit is indicated by an OR gate?

a. Parallel
b. Series parallel
c. Parallel series
d. Series

19. In Boolean algebra, the only numerical values represented are

a. 0 and 1.
b. 0 and 2.
c. 1 and 2.
d. 0 through 8.

20. The truth table may be used in a logical problem to

a. prove the Boolean equation.
b. simplify the problem by complementation.
c. arrive at a summation of the problem.
d. point out the theorem which may be used to solve the problem.

21. The basic purpose of the logic diagram is to

a. illustrate the required functions and type of circuit.
b. aid in construction of the truth table.
c. illustrate the interconnection of indicated circuits.
d. aid in the simplification of the Boolean equation.

8

22. Boolean algebra is useful in representing

a. algebraic functions.
b. switching actions.
c. binary notation.
d. trigonometric relations.

23. To turn on a light (X), we must have switch (D) or switch (E) turned on. Which equation and truth table apply?

a.

D	E	X
0	0	0
0	1	0
1	0	0
1	1	1

$D \cdot E = X$

b.

D	E	X
0	0	0
0	1	0
1	0	0
1	1	1

$D + E = X$

c.

D	E	X
0	0	0
0	1	1
1	0	1
1	1	1

$D + E = X$

d.

D	E	X
0	0	0
0	1	1
1	0	1
1	1	1

$D \cdot E = X$

24. In a 2-story house, a switch (A) at the top of the stairs and another switch (B) at the bottom of the stairs control the staircase light (C). The circuit is connected so light (C) will be on only when both switches are in the same position. Derive the equation for this circuit, using a truth table.

a. $A\overline{B} + \overline{A}B = C$
b. $\overline{A}\,\overline{B} + AB = C$
c. $(\overline{A} + \overline{B})(A + B) = C$
d. $(\overline{A} + B)(A + \overline{B}) = C$

Total Points: 24

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FUNDAMENTALS OF DIGITAL LOGIC

Lesson 3

Logic Gates

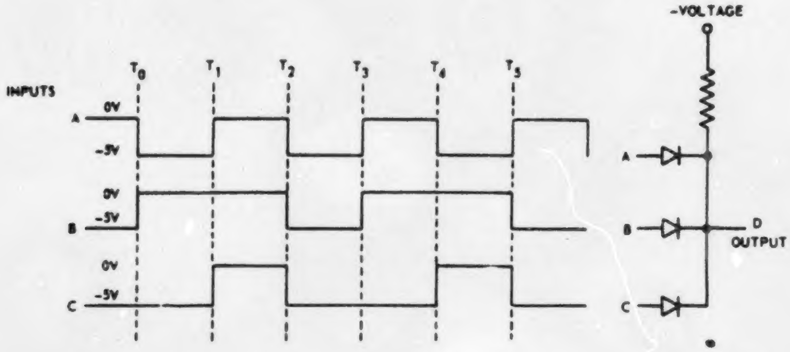
STUDY ASSIGNMENT: MCI 28.6d, Fundamentals of Digital Logic, chap 3.

WRITTEN ASSIGNMENT:

A. Multiple Choice: Select the ONE answer which BEST completes the statement or answers the question. After the corresponding number on the answer sheet, blacken the appropriate box.

Value: 1 point each

Note: Questions 1-4 refer to this figure.



1. If 1 is represented by the relatively low level, the circuit is a(an)_____gate.

   a. OR
   b. NOR
   c. NAND
   d. AND

2. If 1 is represented by the relatively high level, the circuit is a(an)_____gate.

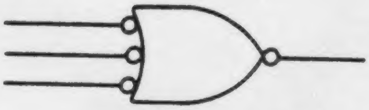
   a. OR
   b. AND
   c. NOR
   d. NAND

3. The output will be —5 volts between times

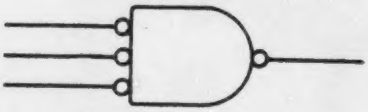
   a. T_0 and T_1.
   b. T_1 and T_2.
   c. T_2 and T_3.
   d. T_3 and T_4.

4. The logic symbol for the circuit is

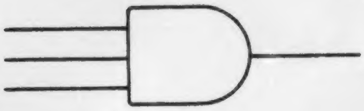
A.



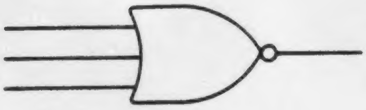
B.



C.



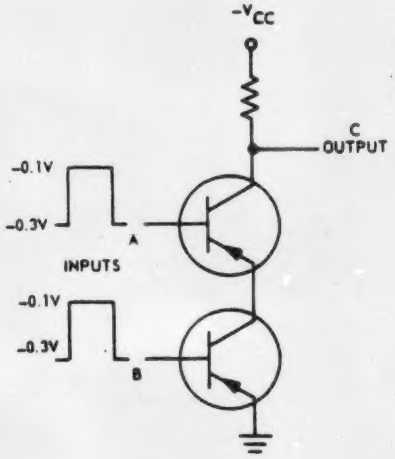
D.



5. How many stable states must a circuit have to be used as a logic element in digital equipment?

a. 1
b. 2
c. 3
d. 4

Note: Questions 6-8 refer to this figure.



6. If the inputs at A and B are -0.3 volt at the same time, the output at C is

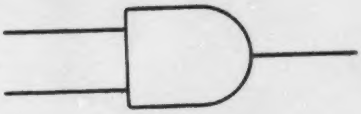
a. -0.1 volt.
b. -0.3 volt.
c. -0.4 volt.
d. $-V_{CC}$.

7. If the -0.3-volt level represents 1, the circuit is a(an)

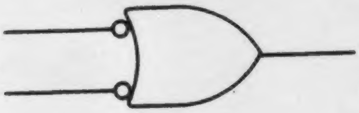
a. AND gate.
b. NOR gate.
c. positive input OR gate with inversion.
d. negative input AND gate with inversion.

8. The logic symbol for the circuit is

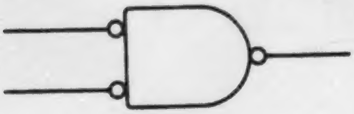
A.



B.



C.



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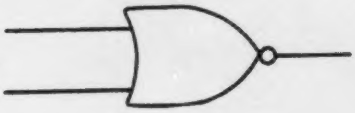


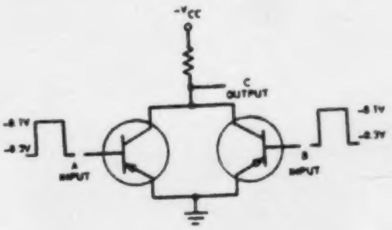
9. The Boolean equation for an EXCLUSIVE OR function is

a. $\underline{A} + \underline{B} = C$
b. $\bar{A} + \bar{B} = C$
c. $\bar{A}\underline{\bar{B}} + \underline{A}B = C$
d. $A\bar{B} + \bar{A}B = C$

10. The output of a logic switching circuit is an electrical signal which represents

a. 1.
b. 0.
c. a complement.
d. a logical conclusion.

Note: Questions 11-14 refer to this figure.



11. The circuit is an example of a _____ logic circuit.

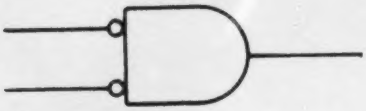
a. direct-coupled transistor
b. positive
c. resistor-transistor
d. negative

12. If the –0. 3-volt level represents a 1, the circuit is a(an)

a. OR gate.
b. AND gate.
c. AND gate with inversion.
d. NOR gate with inversion.

13. The logic symbol for the circuit is

A.



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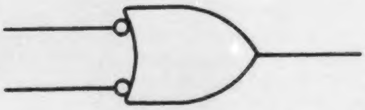

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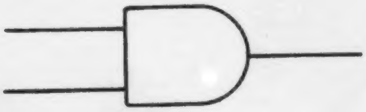

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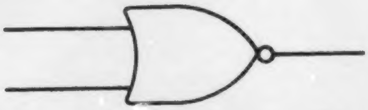

28. 6
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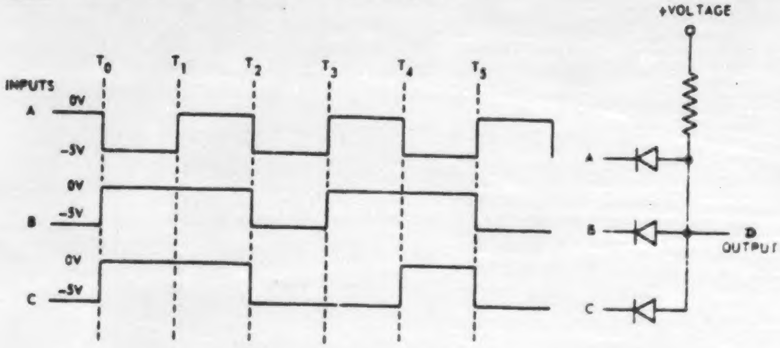
14. If the inputs at A and B are −0.3 volt at the same time, the output at C is

a. −0.1 volt.
b. −0.3 volt.
c. −0.4 volt.
d. $-V_{cc}$.

15. In a diode positive OR or negative AND gate, the _____ would be connected to the _____.

a. load resistor -- power source.
b. anodes of the diodes -- load resistor.
c. load resistor -- positive power source.
d. anodes of the diodes -- output.

Note: Questions 16-19 refer to this figure.



16. If 1 is represented by a relatively low level, the circuit is a(an) _____ gate.

a. OR
b. AND
c. NOR
d. NAND

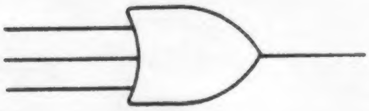
17. If 1 is represented by a relatively high level, the circuit is a(an) _____ gate.

a. OR
b. AND
c. NOR
d. NAND

18. The output will be 0 volts between times

a. T_3 and T_4.
b. T_2 and T_3.
c. T_1 and T_2.
d. T_0 and T_1.

19. The logic symbol for the circuit is

A.


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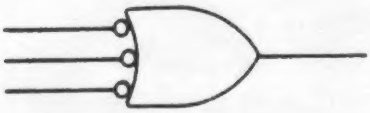

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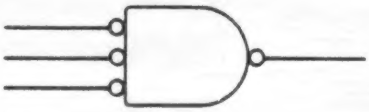

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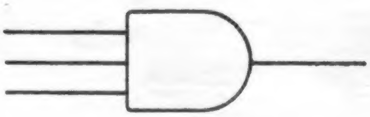
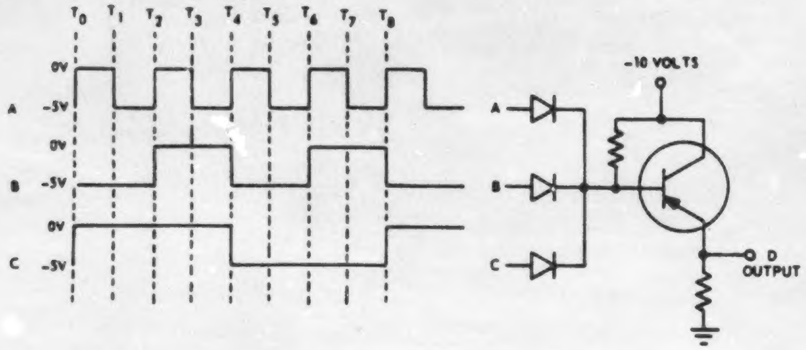


Note: Questions 20-24 refer to this figure.



20. The output voltage is −5 volts between times

a. T_1 and T_2.
b. T_3 and T_4.
c. T_5 and T_6.
d. T_7 and T_8.

21. The circuit is an example of a _____ logic circuit.

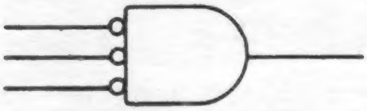
a. direct-coupled
b. diode-and-transisto-
c. resistor-transistor
d. diode

22. Between times T_2 and T_4 the output voltage is

a. 0 volts.
b. +5 volts.
c. −5 volts.
d. $-V_{cc}$.

23. The logic symbol for the circuit is

A.



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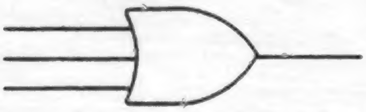

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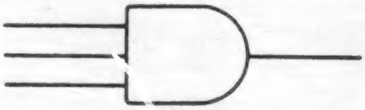

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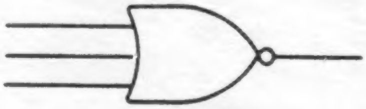


24. If the 0-level represents 1, the circuit is a(an)_____gate.

a. NAND
b. AND
c. OR
d. NOR

25. The circuit for a positive AND gate is the equivalent circuit for a(an) _____ gate.

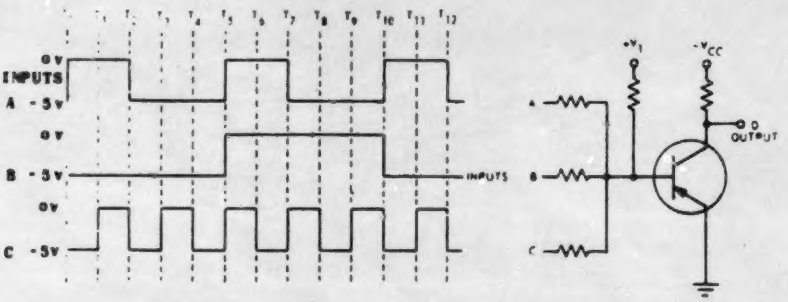
a. positive OR
b. NOR
c. EXCLUSIVE OR
d. negative OR

26. In a diode AND or negative OR gate, the _____ would be connected to the _____.

a. load resistor -- negative power source
b. cathodes of the diodes -- load resistor
c. load resistor -- positive power source
d. cathodes of the diodes -- output

28. b
lan 3; p. 5

Note: Questions 27-30 refer to this figure.


T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
0 V
INPUTS
A -5 V
0 V
B -5 V
INPUTS
0 V
C -5 V
+V1
-VCC
A
B
C
D
OUTPUT

27. The circuit is an example of a _____ logic circuit.

a. diode
b. resistor-transistor
c. diode-and-transistor
d. direct-coupled

28. The output voltage is –5 volts between times

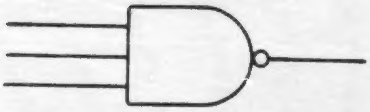
a. T_0 and T_3.
b. T_4 and T_3.
c. T_5 and T_6.
d. T_6 and T_7.

29. If the 0-volt level represents 1, the circuit is a(an)

a. OR gate.
b. AND gate.
c. AND gate with inversion.
d. NOR gate with inversion

30. The logic symbol for the circuit is

A



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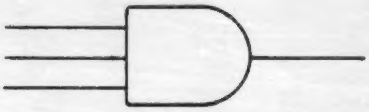

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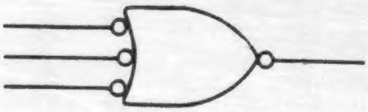

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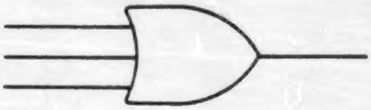

Total Points: 30

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28.6d

FUNDAMENTALS OF DIGITAL LOGIC

Lesson 4

Logic Flip-Flops; Nonlogic Circuits; Magnetic Cores

STUDY ASSIGNMENT: MCI 28.6d, Fundamentals of Digital Logic, chaps 4, 5, and 6.

WRITTEN ASSIGNMENT:

A. Multiple Choice: Select the ONE answer which BEST completes the statement or answers the question. After the corresponding number on the answer sheet, blacken the appropriate box.

Value: 1 point each

1. In the circuit shown in figure 4-2 in your textbook, when Q1 is conducting, the output of Q2 will be

   a. more negative than the output of Q1.
   b. at its relatively high stable state.
   c. a square wave.
   d. almost 0 volts.

2. In the input circuits of a complementing flip-flop, illustrated in figure 4-5 in your textbook, the purpose of the steering diodes is to

   a. obtain delayed switching time.
   b. insure that only one transistor conducts at a time.
   c. bring the cutoff transistor into conduction.
   d. insure that the input triggering signal is felt on only one transistor at a time.

3. In figure 4-6 in your textbook, Q1 will always be brought into conduction by a trigger that is applied to

   a. point B.
   b. point C only.
   c. points C and D simultaneously.
   d. point A.

4. If the circuit shown in figure 4-8 in your textbook is used in a circuit having positive logic (relatively high voltage represents a 1) and Q4 is conducting, the flip-flop is

   a. in the ZERO state.
   b. inverting the level of logic.
   c. in the ONE state.
   d. not in a stable condition.

5. The emitter follower uses the _____ configuration.

   a. common-emitter
   b. common-collector
   c. common-base
   d. grounded-emitter

6. If an LC delay line has six sections and each consists of an inductor of 2.5 microhenrys and a capacitor of 250 microfarads, the total delay is _____ microseconds.

   a. 1.5
   b. 15.0
   c. 150.0
   d. 175.0

7. A complementary emitter-follower configuration is used to

   a. invert the logic levels of the input pulse.
   b. produce the 1's complement of the input.
   c. trigger a complementing flip-flop.
   d. give fast rise and fall times to the output pulse.

8. One of the principal uses of an emitter follower is as a(an)

   a. voltage amplifier.
   b. phase inverter.
   c. impedance-matching device.
   d. pulse-shaping device.

9. An inverter circuit performs the _____ function.

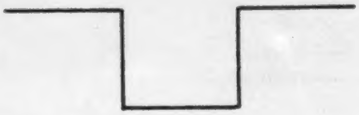
   a. OR
   b. AND
   c. NOT
   d. EXCLUSIVE OR

10. In figure 5-4 in your textbook, how long will the secondary of T1 have current flow through it?

    a. For the duration of the input pulse
    b. As long as the primary of T1 has current flow through it
    c. Until capacitor C3 discharges
    d. Until the current through Q1 reaches its maximum

11. Identify the waveform of the base voltage of Q3 (V_{b3}) in figure 5-10 in your textbook.

A.



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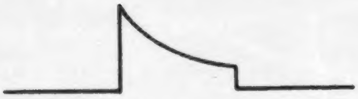

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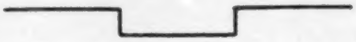

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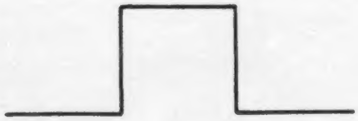


12. If the relay driver shown in figure 5-5 in your textbook is used in a negative logic circuit, a 1 input causes

    a. current to flow through K1.
    b. CR1 to conduct.
    c. the base of Q1 to be at a positive potential.
    d. the relay to deenergize.

13. The output of a Schmitt trigger circuit is always a _____ wave.

    a. sine
    b. sawtooth
    c. rectangular

14. For signal delays of more than several hundred nanoseconds, the computer manufacturer finds the use of LC delay lines impractical because of their

    a. current rating.
    b. voltage rating.
    c. physical size.
    d. characteristic impedance.

15. How many core planes are required to store 32 words of 16 digits each?

    a. 16
    b. 32
    c. 48
    d. 512

16. To write a binary 1 into a ferrite core used in a coincident current memory, the circuit applies

a. full-current pulses simultaneously to the X and Y drive wires.
b. half-current pulses simultaneously to the X and Y drive wires.
c. a full-current pulse to the X drive wire and a half-current pulse to the Y drive wire.
d. a full-current pulse to the Y drive wire and a half-current pulse to the X drive wire.

17. The path of the B-H curve as a material is saturated in one direction. demagnetized, saturated in the opposite direction, and finally returned to the initial point of saturation is called a

a. hysteresis loop.
b. retentivity curve.
c. saturation loop.
d. magnetization curve.

18. To read from a ferrite core, all of the following wires are used EXCEPT the_____wire.

a. sense
b. inhibit
c. X drive
d. Y drive

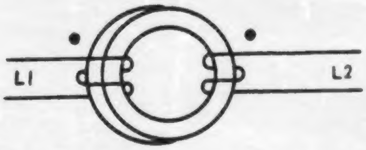
19. [illegible] figure 6-5 in your textbook, the function of CR1 in the transfer loop is to

a. dampen oscillations of L2.
b. prevent premature switching of core B.
c. prevent premature switching of core A.
d. allow current always to enter the nondot side of L2.

20. During the write tunction, all of the following wires in the ferrite core are used EXCEPT the _____ wire.

a. sense
b. inhibit
c. X drive
d. Y drive

Note: Questions 21 and 22 refer to this figure.



21. Assume that the metallic ribbon core is in the ONE state. Current flow into the dot side of L1 causes the core to

a. switch to the ZERO state.
b. remain in the ONE state.
c. induce a large output voltage across L2.
d. be magnetized in a counterclockwise direction.

22. When the current switches to a ZERO state, it causes

a. a positive polarity at the dot side of L2.
b. the core to switch to the ONE state.
c. a negative polarity at the dot side of L2.
d. a positive polarity at the nondot side of L1.

23. A change in the state of a ferrite core is brought about by

    a. applying a half-current pulse to the sense wire.
    b. applying a half-current pulse to the inhibit wire.
    c. the coincidence of two full-current pulses.
    d. the coincidence of two half-current pulses.

24. A magnetic core makes a good bistable device for storing binary 1 and binary 0 because it

    a. has low retentivity.
    b. requires two half-current pulses to change its state.
    c. can be magnetized in either of two directions.
    d. is made of ferrite.

Total Points: 24

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28.6d

FUNDAMENTALS OF DIGITAL LOGIC

Lesson 5

Logic Circuits

STUDY ASSIGNMENT: MCI 28.6d, Fundamentals of Digital Logic, chap 7.

WRITTEN ASSIGNMENT:

A. Multiple Choice: Select the ONE answer which BEST completes the statement or answers the question. After the corresponding number on the answer sheet, blacken the appropriate box.

Value: 1 point each

1. The maximum number of pulses that a 5-stage binary counter can count and present is

   a. 31.
   b. 32.
   c. 63.
   d. 64.

2. The maximum decimal count that a 6-stage binary counter can contain is

   a. 31.
   b. 32.
   c. 63.
   d. 64.

3. In a 4-stage serial up-counter made up of flip-flops A, B, C, and D, with flip-flop A as the LSD, you would expect

   a. flip-flop C to change state on every other input pulse.
   b. flip-flop C to change state when flip-flop B changes from the ONE to the ZERO state.
   c. flip-flop B to change state when flip-flop A changes from the ZERO to the ONE state.
   d. flip-flop D to change state when flip-flop C changes state.

4. A serial down-counter may be changed to a serial up-counter by

   a. adding AND gates.
   b. adding OR gates.
   c. using the flip-flop's ONE output.
   d. using the flip-flop's ZERO output.

5. Compared with a serial counter, a parallel counter is

   a. simpler.
   b. longer.
   c. slower.
   d. faster.

6. The minimum number of flip-flops needed for a parallel counter is

   a. 2.
   b. 4.
   c. 8.
   d. 10.

7. In a 3-stage ring counter, the number of stages in the ZERO state simultaneously is

   a. 3.
   b. 2.
   c. 1.
   d. 0.

8. The principal methods of information transmission are

a. parallel and redundant.
b. series and redundant.
c. parallel and serial.
d. series and lateral.

9. Registers are used primarily for

a. counting, adding, and shifting.
b. counting, adding, and storage.
c. adding, storage, and shifting.
d. storage, shifting, and counting.

10. Assume that 00100100 is placed in an 8-stage shift register and that the machine is instructed to divide it by 4. When the operation is complete, the shift register will contain

a. 00001001.
b. 10010000.
c. 00010010.
d. 00100100.

11. Assume that 001011 is placed in a 6-stage binary shift register and that the machine is instructed to multiply it by 2. When the operation is complete, the shift register will contain

a. 010101.
b. 010011.
c. 010110.
d. 010111.

12. A full adder consists of two

a. half-adders.
b. half-adders and an OR gate.
c. OR gates.
d. OR gates and a half-adder.

13. A shift register divides a binary number by 4 by shifting the bits _____ place(s) to the _____.

a. 1--left
b. 1--right
c. 2--left
d. 2--right

14. The purpose of the adder circuit is to perform

a. logical addition.
b. the product of sums.
c. the sum of products.
d. binary addition.

15. How many sum combinations of two bits are possible?

a. 1
b. 2
c. 3
d. 4

16. How many bits can the full-adder circuit sum?

a. 3
b. 4
c. 5
d. 6

17. A parallel adder capable of handling a 6-bit binary word consists of

a. 6 full adders.
b. 6 half-adders.
c. 5 full adders and a half-adder.
d. 5 half-adders and a full adder.

18. Which is the Boolean equation for a logic circuit that will detect a count of $\overline{9}$ from a counter made up of flip-flops A, B, C, and D (LSD is flip-flop A)?

a. $9 = A\,\overline{B}\,\overline{C}\,D$
b. $\overline{9} = \overline{A}\,B\,C\,\overline{D}$
c. $\overline{9} = A + \overline{B} + \overline{C} + D$
d. $\overline{9} = \overline{A} + B + C + \overline{D}$

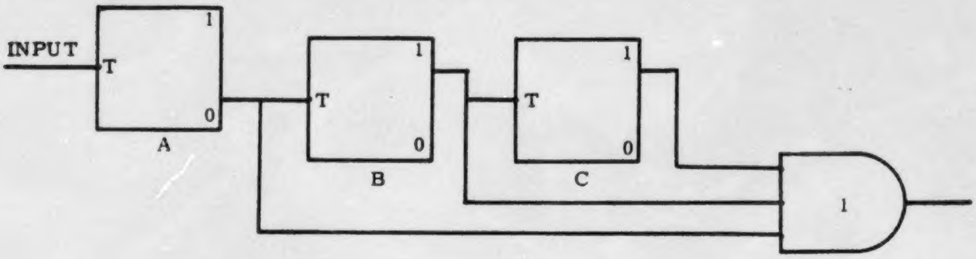
19. Which is the Boolean equation for a logic circuit that will detect a count of 14 from a counter made up of flip-flops A, B, C, and D (LSD is flip-flop A)?

a. $14 = \overline{A} + B + C + D$	c. $14 = \overline{A}\,B\,C\,D$
b. $14 = A\,\overline{B}\,\overline{C}\,\overline{D}$	d. $14 = A + \overline{B} + \overline{C} + \overline{D}$

20. A combination of switching circuits used to translate two or more signals into one output signal is called a(an)

a. decoder.	c. coder.
b. encoder.	d. converter.

21. Which binary number will be detected by the decoder shown below?



a. 001	c. 110
b. 100	d. 011

22. A multiple-output switching network that produces a different single-output signal for each different input or combination of input signals is called a(an)

a. converter.	c. matrix.
b. encoder.	d. coder.

23. Refer to figure 7-21 in your textbook. What will be the approximate output voltage if binary 4 is applied to the input?

a. 5	c. 20
b. 10	d. 30

24. A resistor ladder type of digital-to-analog converter is connected to a 6-stage counter, and the applied voltage to the ladder is 126 volts. What is the output voltage of the network when the count in the counter is 47?

a. 94	c. 101
b. 95	d. 102

25. In a ramp-voltage encoder, the counter starts counting when the

a. start pulse resets it.
b. analog voltage exceeds zero.
c. ramp voltage exceeds zero.
d. ramp voltage exceeds the analog voltage.

Total Points: 25

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